

S/M No. : OSDPC72001

Service Manual

(7.0-Inch) LCD Color Monitor &
DVD Player

Model: DPC-7200PD



✓ Caution

: In this Manual, some parts can be changed for improving, their performance without notice in the parts list. So, if you need the latest parts information, please refer to PPL(Parts Price List) in Service Information Center

DAEWOO 
ELECTRONICS

MAY. 2005

CONTENTS



Specification.....	3
Block Diagram.....	5
General Alignment Instruction.....	7
Troubleshooting.....	8
Printed Circuit Board.....	10
IC Block Diagram and Lead Identification.....	16
Explode View.....	31
Schematic Diagram.....	32

SPECIFICATION

LCD MONITOR

Model No.: LMD-4708GQU

Out put: 50mW/16ohm

Supply Voltage: _____

Description		Condition	Unit	Limit	Nominal				
Headphone Output		1KHz 0dB	mW	3±2	3				
Headphone Noise		No Signal	mV	<1mV	<1mV				
SPK MAX Output	L	1KHz 0dB	mW	600±100	600				
	R	1KHz 0dB	mW	600±100	600				
SPK MAX Output(AV IN)	L	1KHz 0dB	mW	600±100	600				
	R	1KHz 0dB	mW	600±100	600				
REF THD		1KHz 0dB	%	5	3				
SPK S/N		Infinity zero/-∞ dB/L&R	dB	≥35	≥35				
Headphone S/N		Infinity zero/-∞ dB/L&R	dB	≥60	≥60				
Luminance(MAX)		White Signal	LUX	300±50	300				
Luminance(8STEP)		White Signal	LUX	250±50	250				
Luminance(MIN)		White Signal	LUX	100±50	100				
Headphone RESP	L	20Hz	dB	±3	0				
		125Hz	dB	±3	0				
		10KHz	dB	±3	0				
		20KHz	dB	±3	0				
	R	20Hz	dB	±3	0				
		125Hz	dB	±3	0				
		10KHz	dB	±3	0				
		20KHz	dB	±3	0				

DVD

Model No.: LMD-4708GQU

Out put: 50mW/16ohm

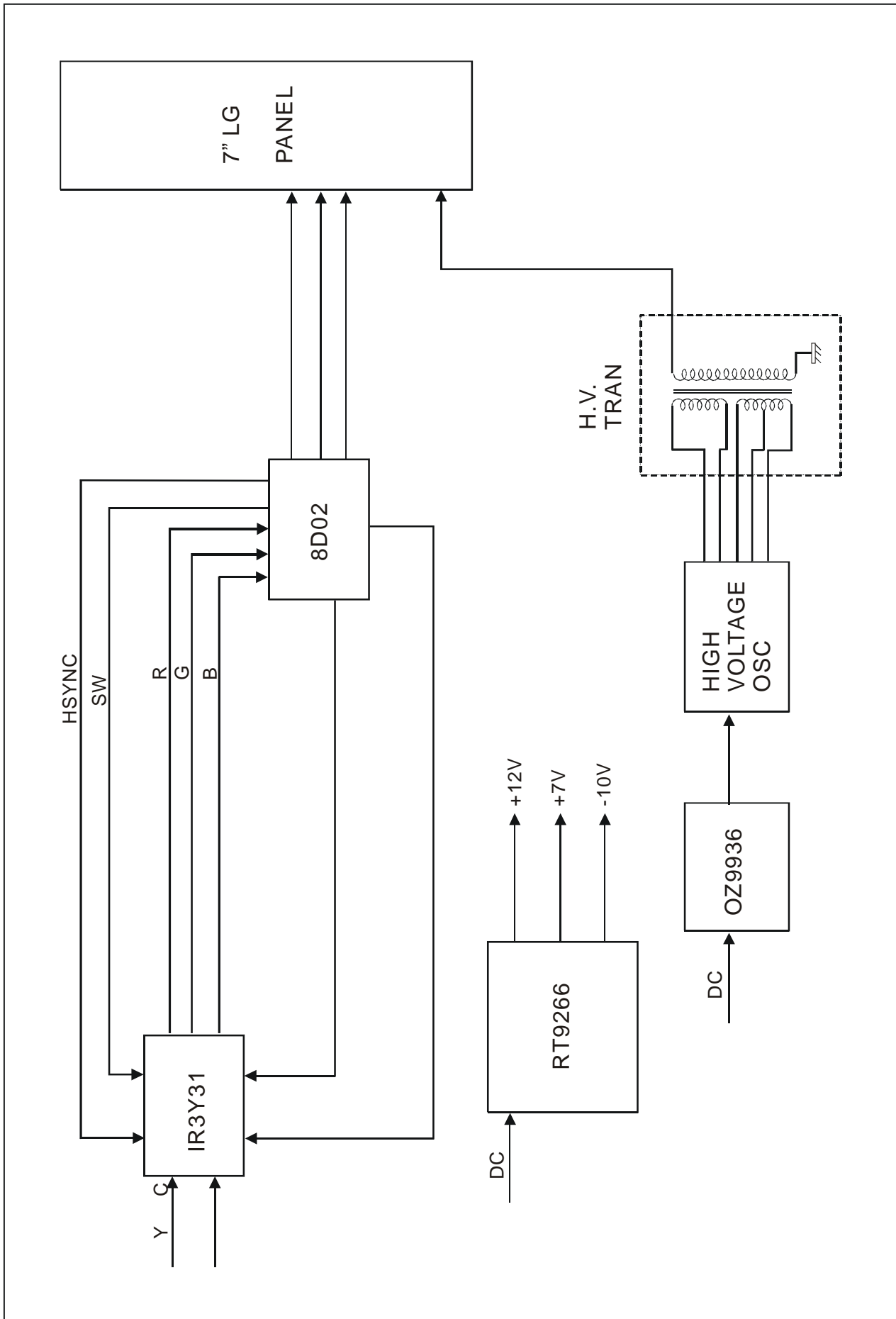
Supply Voltage: _____

Description		Condition	Unit	Limit	Nominal				
Video Signal Level		75% color bar/75ohm	Vp-p	0.7±0.1	0.7				
SYNC Level			Vp-p	0.3±0.1	0.3				
Video out level			Vp-p	1.0±0.2	1				
Video out level(Unload)		75% color bar	Vp-p	2.0±0.2	2				
Audio out level	CD	1KHz/0dB/10K	V	2.0±0.2	2				
	DVD	1KHz/0dB/10K	V	2.0±0.2	2				
FREQ RESP (DVD) (20Hz~20KHz)		20Hz	dB	≤±3	0				
		125Hz	dB	≤±3	0				
		10KHz	dB	≤±3	0				
		20KHz	dB	≤±3	0				
Signal-to-noise radio		Infinity zero/-∞ dB/L&R	dB	≥60	≥60				
Audio distortion&noise (DVD)		1KHz/0dB/L&R	dB	≤-65	-65				
Dynamic range (DVD)		1KHz/-60dB	dB	≥85	≥85				
R/L Cross sound (DVD)		1KHz/0dB/L&R	dB	≥45	≥45				
1KHz Channel unbalance (DVD)		1KHz/0dB/L&R	dB	≤3	0				
Power Consumption		Standby	W	0	0				
DC 9V		Rating	W	≤12	≤12				
ECC Entircity		A BEX TDV-552	um	≥100	100				
Scratch		A BEX TDV-541	mm	≥1.6	1.6				
Black dot		A BEX TDV-545	mm	≥φ0.8	0.8				
Finger Print		A BEX TDV-545	um	≥φ65	65				
Vertical deviation		A BEX TDV-533	mm	≥0.6	0.6				

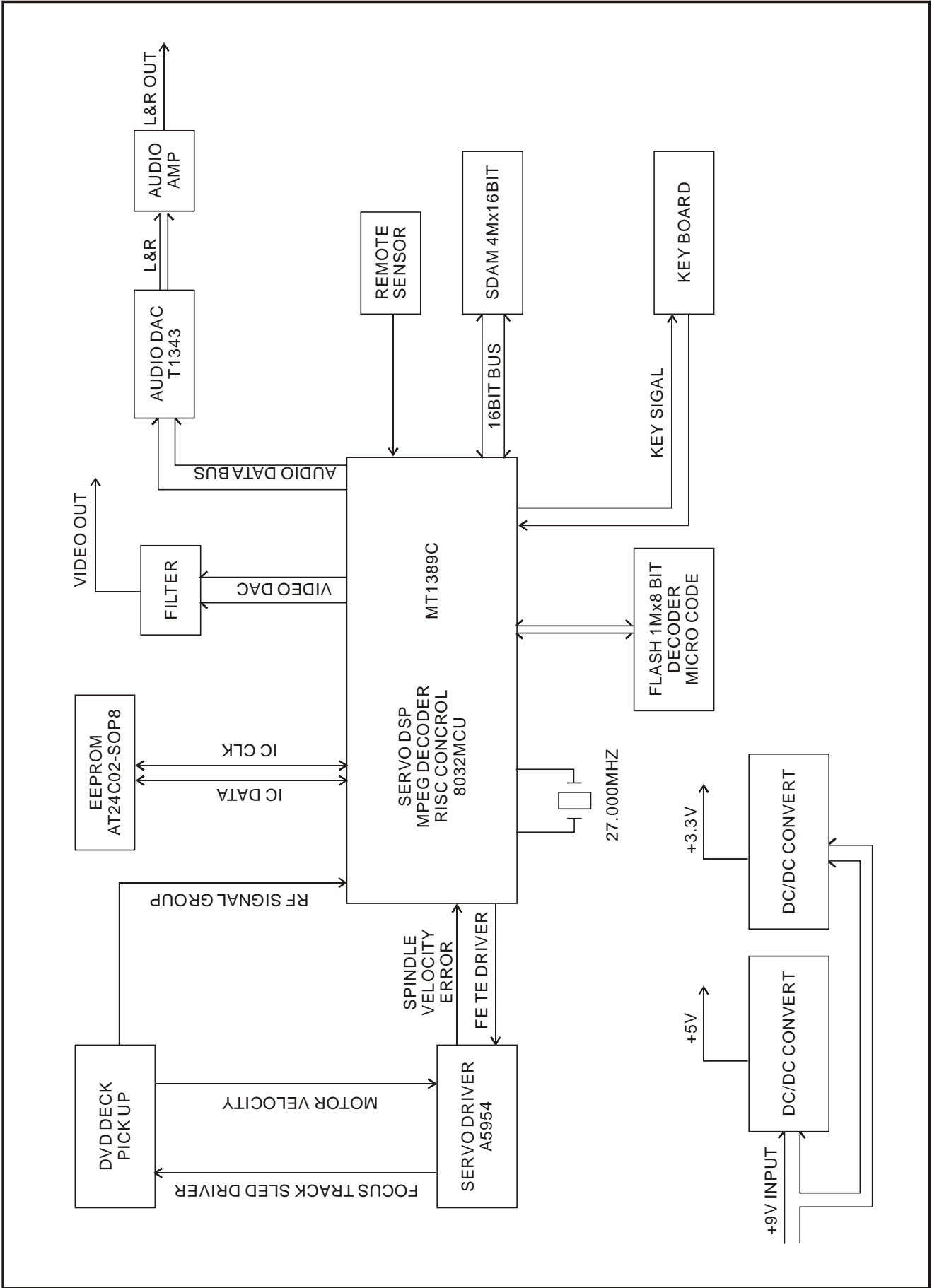
Note: Nominal specs represent the design specs. All units should be able to approximate these. Some will exceed and some may drop slightly below these specs. Limit specs represent the absolute worst condition that might still be considered acceptable. In no case should a unit fail to meet limit specs.

BLOCK DIAGRAM

LCD



DVD



GENERAL ALIGNMENT INSTRUCTION

The Main PCB of Monitor Modification:

1. Input voltage is 6.8V-16V, input signal is test circuit BY 5418.
2. Adjust VRT5 to get test point: 15720Hz..
3. Adjust VRT4 to get horizontal phase shift.
4. Adjust VRT1 to get good performance.
5. Adjust S201. S202 to get good Tint.

The main PCB of DVD Modification:

1. Adjust the brightness to the brightest by VR, adjust video pattern's color to white, test the screen
Brightness is 200 ± 102 LUX.
With luminometer You can adjust R69 to get this standard.

TROUBLESHOOTING

LCD

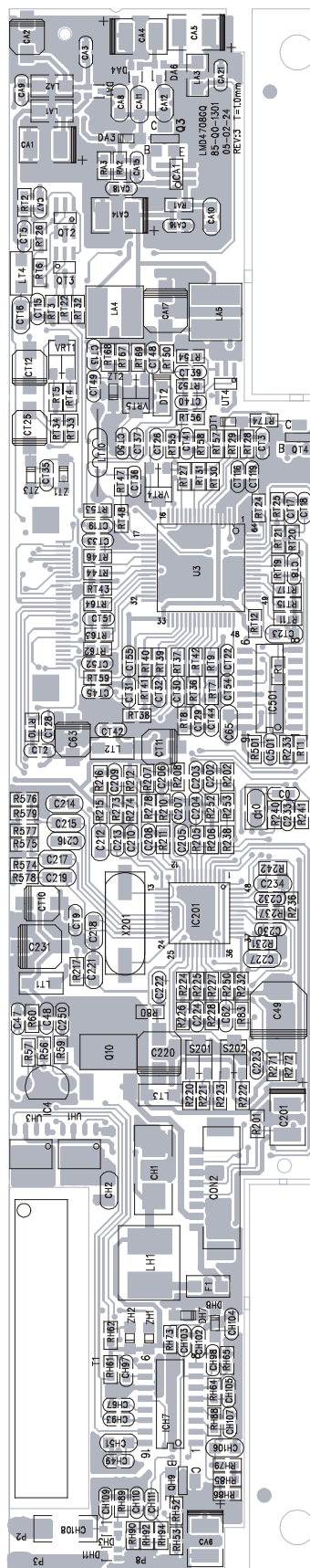
SYMPTOM	CAUSE	REMEDY
LCD MONITOR PART		
1) Picture distortion	& Defective capacitor (C201)	& Replace capacitor C201.
2) No Picture	& Defective IC (IR3Y31).	& Replace IC IR3Y31.
3) No Picture, Picture no Good	& Defective Q7, Q8.	& Replace Q7, Q8.
4) Color is no good	& Defective X201.	& Replace X201.
5) SYNC no good	& Defective IC 8D02.	& Replace IC 8D02.
6) TINT no good	& Defective S201, S202	& Replace S201,S202.
7) NO Picture	& Defective IC RT9266.	& Replace RT9266.
8) Picture no good	& Defective CON1.	& Replace CON1.
9) Brightness no good	& Defective IC M5237 Q10.	& Replace IC M5237 Q10.

DVD

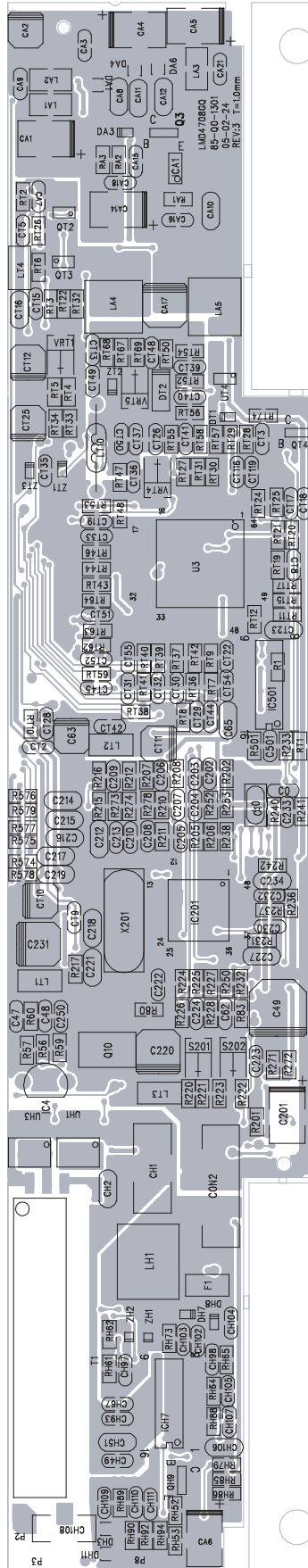
SYMPTOM	CAUSE	REMEDY
DVD PART		
1) No Power	& Power source is not correct. The positive and negative does not match the unit. & Power button defective. & Defective triode U7.	& Replace power source. & Change the position of positive and negative. & Replace power button. & Replace U7.
2) No Picture	& Defective U10 (24C02N). & Defective U5. & Defective IC MTK1389C.	& Replace U10 (24C02N). & Replace U5. & Replace IC MTK1389C.
3) No Sound	& Defective U14 (C4558). & Defective U1 (14053). & Defective U2.	& Replace U14 (C4558). & Replace U1 (14053). & Replace U2.
4) Sound no good	& Defective U14.	& Replace U14.
5) Can not read DISC	& Defective U18. & PICK-up Laser is defective.	& Replace U18. & Replace pick up.
6) No key function	& Defective IC MTK1389C.	& Replace IC MTK1389C.
7) No remote control function	& Defective REMOTE. & Key is Defective.	& Replace REMOTE. & Replace keys.

PRINTED CIRCUIT BOARD

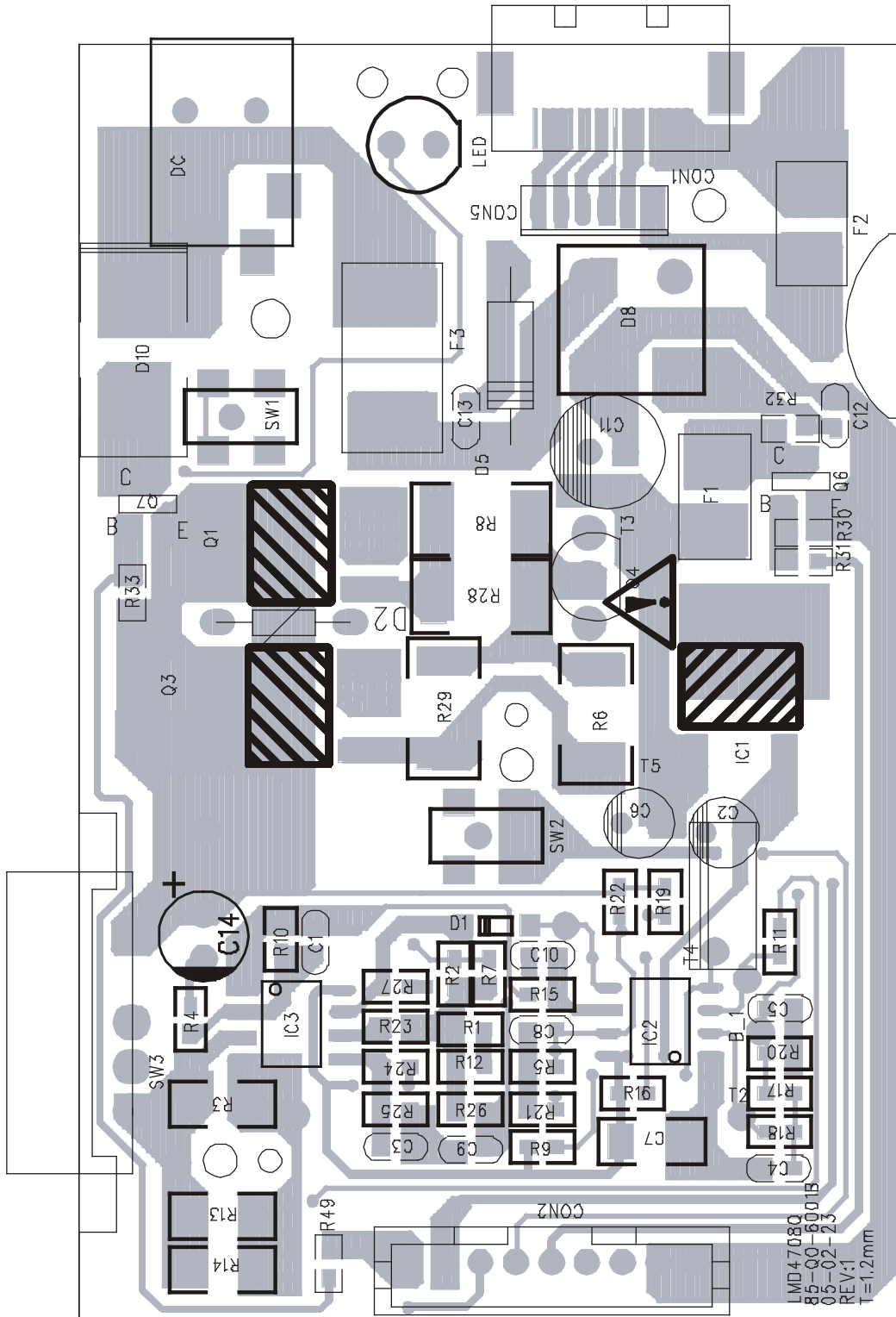
Monitor Main PCB
Top View



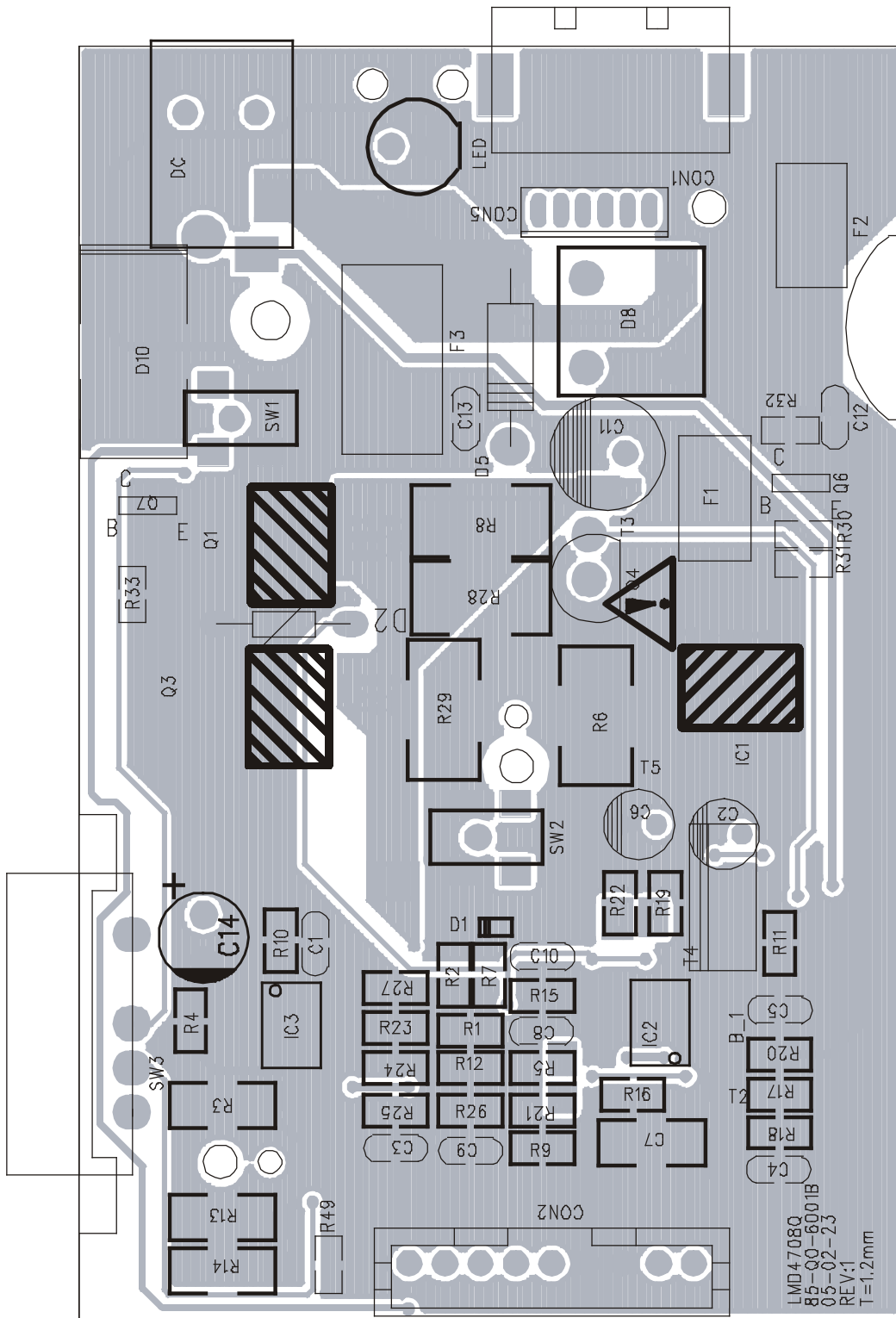
Monitor Main PCB
Bottom View



Battery Charger Circuit PCB Top View

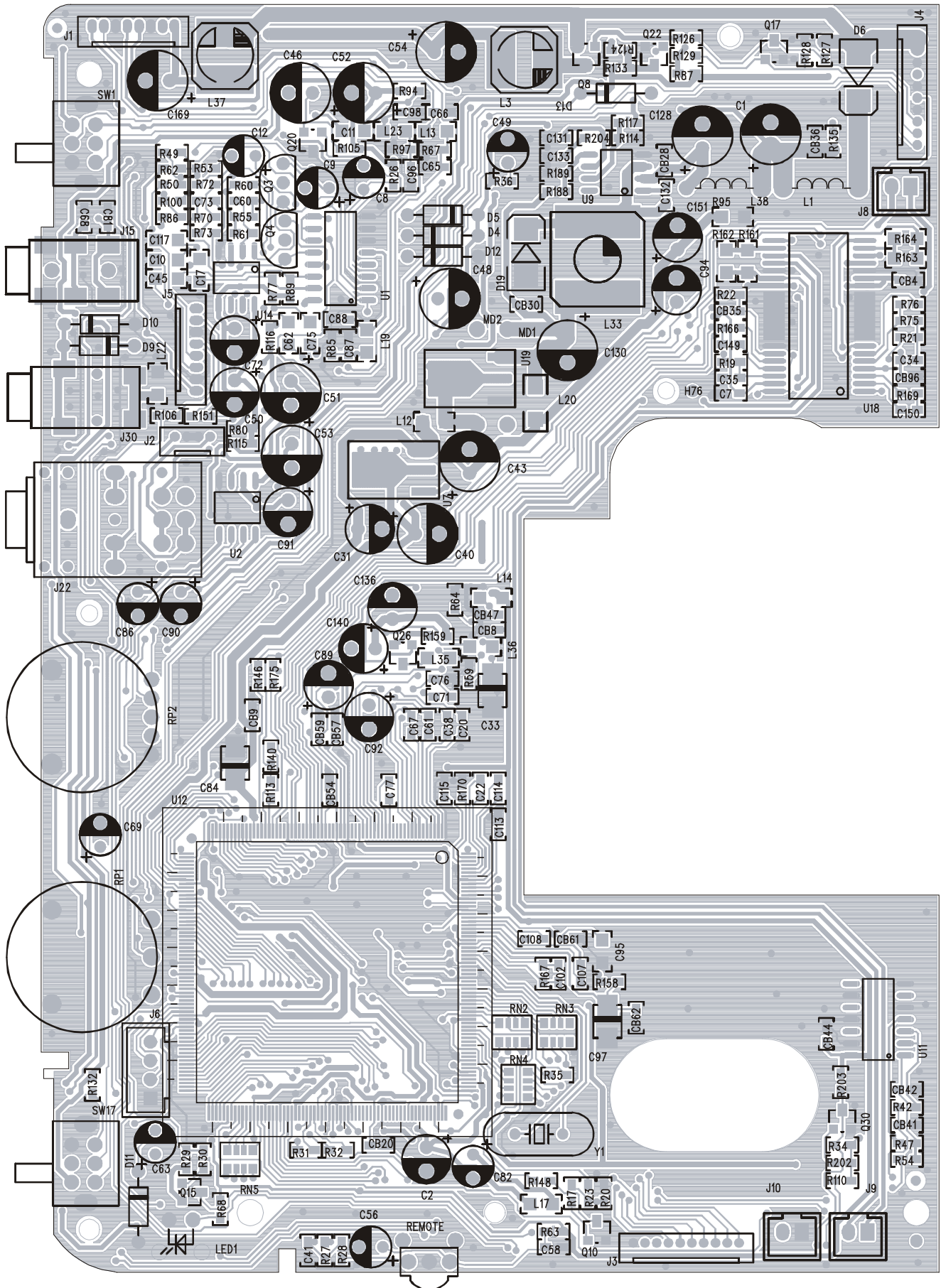


Battery Charger Circuit PCB
Bottom View

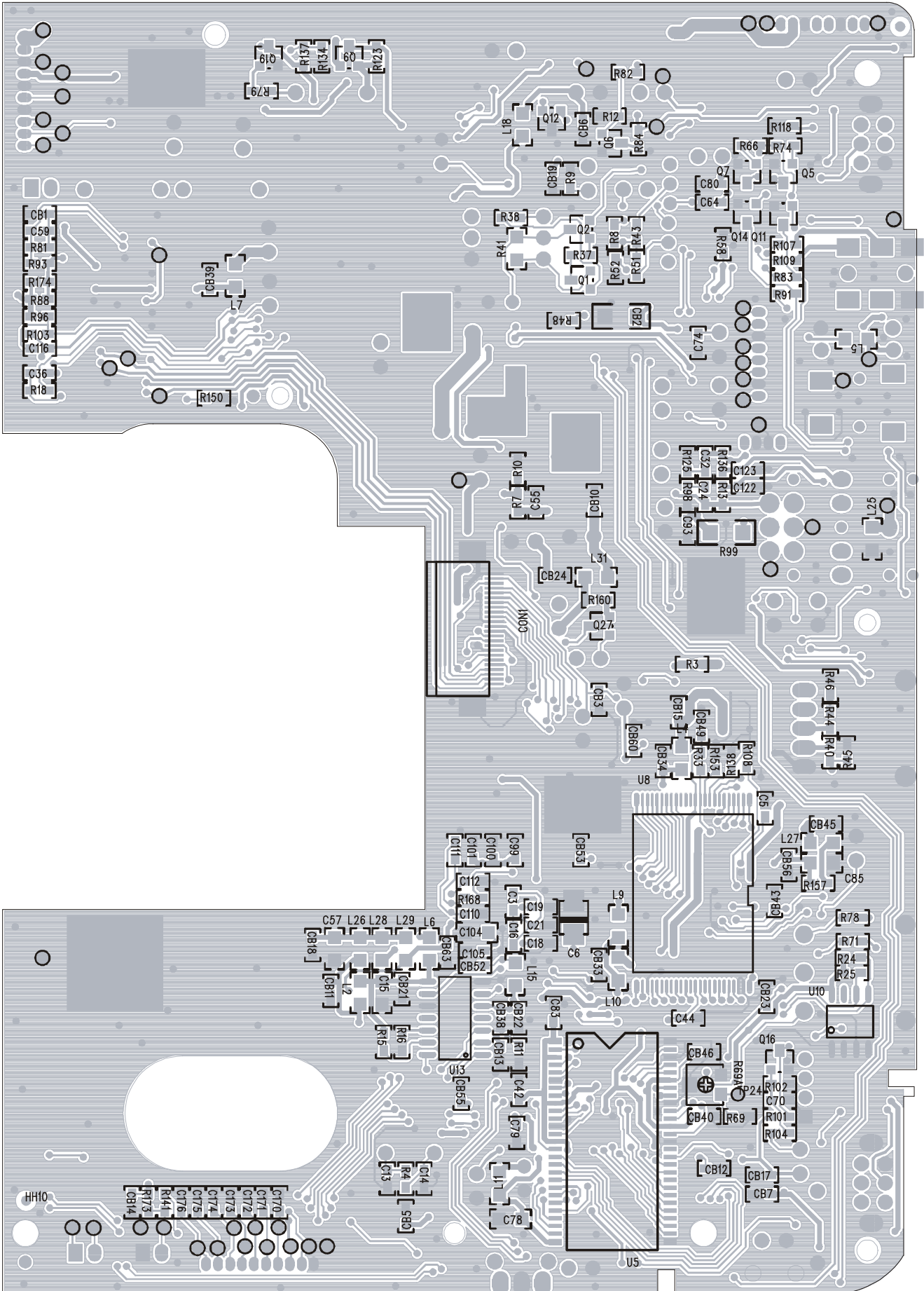


DVD Main PCB

Top View

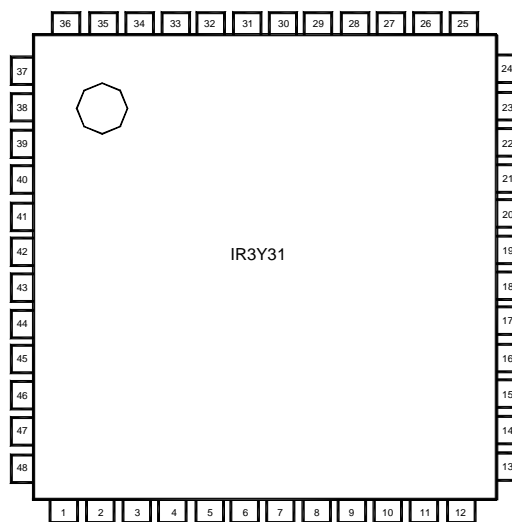
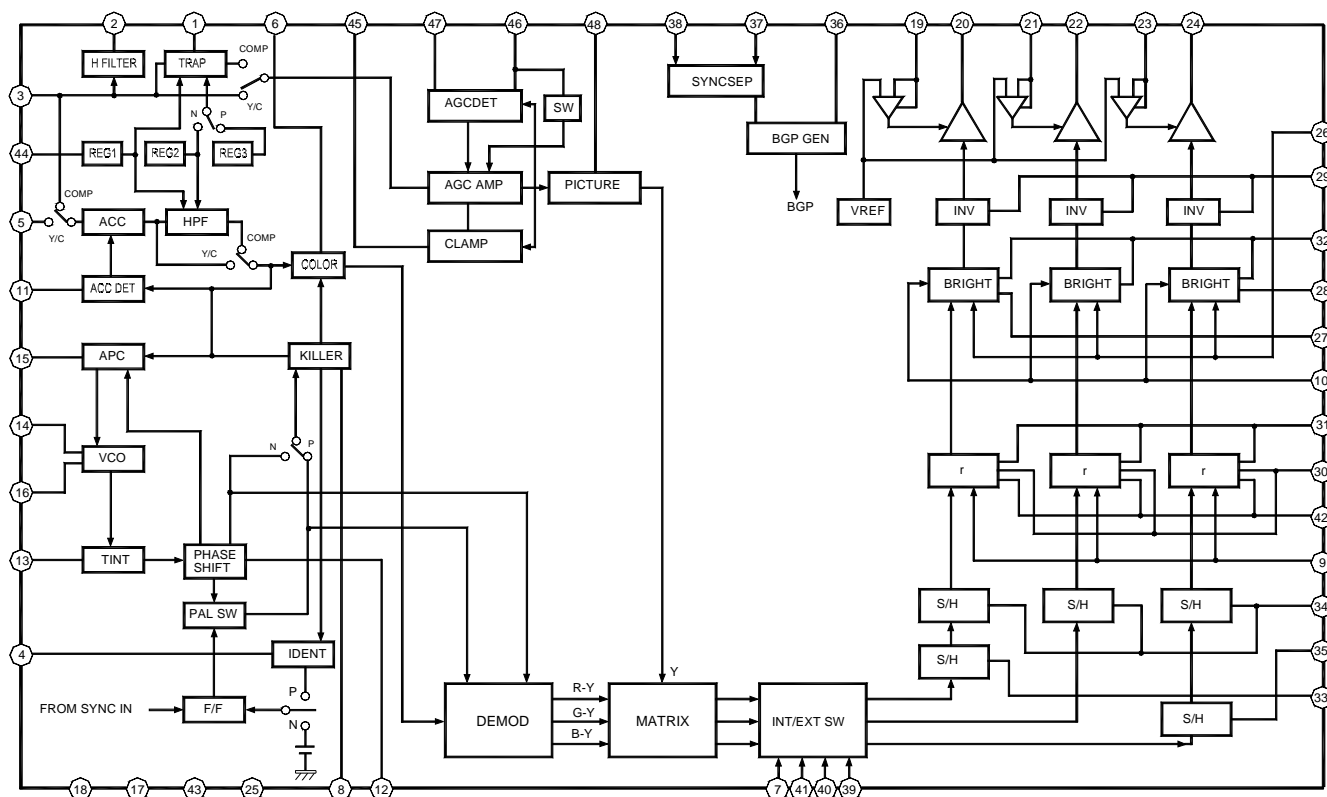


DVD Main PCB
Bottom View



IC BLOCK DIAGRAM & DESCRIPTION

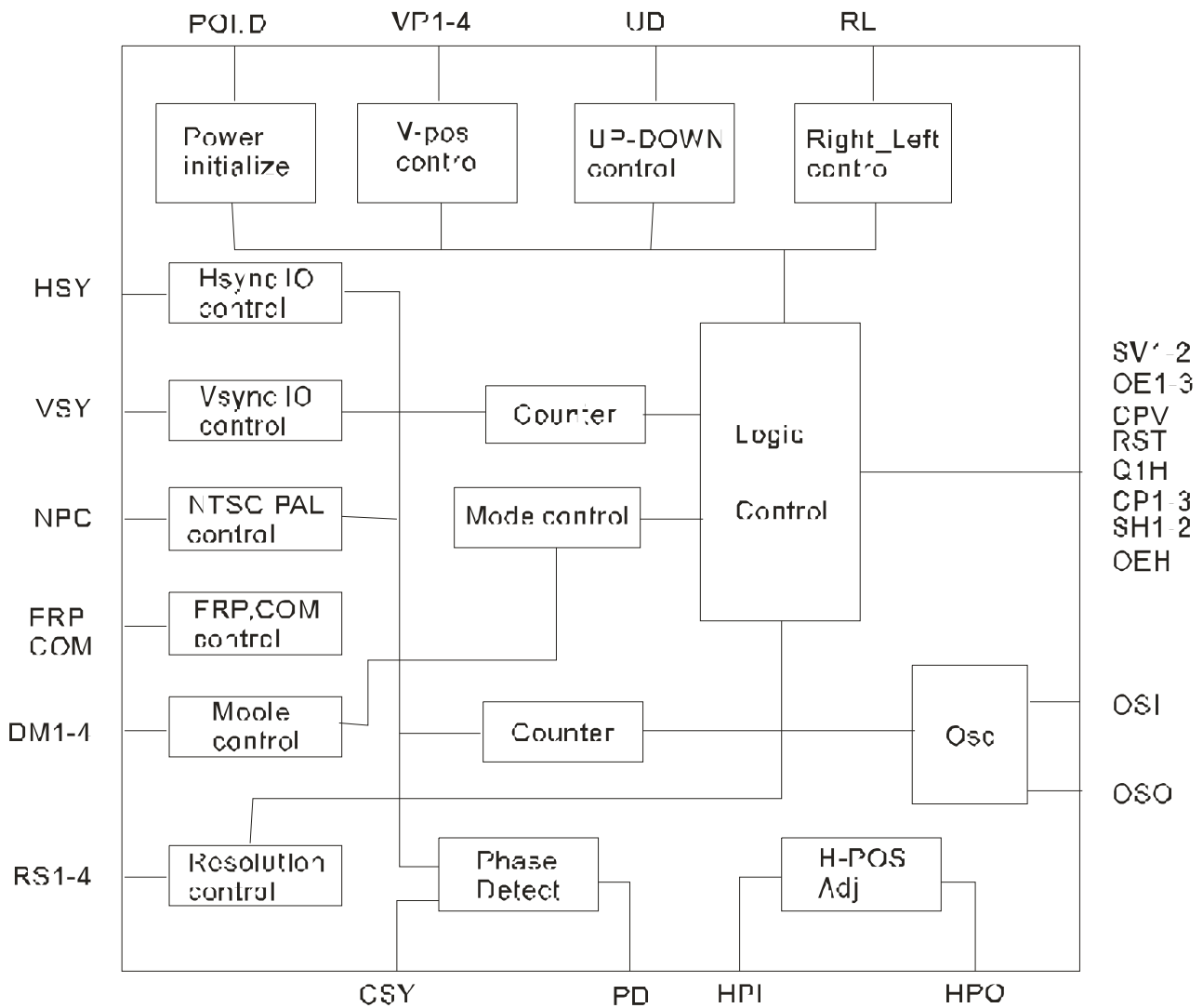
IC IR3Y31



- | | | | |
|-------------------|----------------|------------------|----------------|
| 1. TRAP | 13. TINT | 25. Vcc2 | 37. SYNC OUT |
| 2. H FILTER OUT | 14. VCO IN | 26. BLK | 38. SYNC SEP |
| 3. VIDEO IN | 15. APC FILTER | 27. SUB BRIGHT R | 39. EXT B IN |
| 4. IDENT FILTER | 16. VCO OUT | 28. SUB BRIGHT B | 40. EXT G IN |
| 5. C IN | 17. GND | 29. FRP | 41. EXT R IN |
| 6. COLOR | 18. VEE | 30. GAMMA1 | 42. CONTRAST |
| 7. SW | 19. R DC DET | 31. GAMMA2 | 43. Vcc1 |
| 8. KILLER FILTER | 20. R OUT | 32. BRIGHT | 44. F ADJ |
| 9. PEAK LIMITTER | 21. G DC DET | 33. S/H PULSE R | 45. CLAMP |
| 10. RGB AMPLITUDE | 22. G OUT | 34. S/H PULSE G | 46. AGC FILTER |
| 11. ACC FILTER | 23. B DC DET | 35. S/H PULSE B | 47. AGC OUT |
| 12. R-Y/B-Y PHASE | 24. B OUT | 36. SYNC IN | 48. PICTURE |

IC BLOCK DIAGRAM & DESCRIPTION

IC 8D02C



64 PIN FUNCTION DESCRIPTION - 1				
Pin	Name	I/O	Description	Remark
1	VCC		Power supply	Note 1
2	CSY	I	Composite sync. Input pin	
3	RS4	I	Resolution mode setting pin 4	Note 2
4	RS3	I	Resolution mode setting pin 3	Note 2
5	RS2	I	Resolution mode setting pin 2	Note 2
6	RS1	I	Resolution mode setting pin 1	Note 2
7	DM4	I	Display mode setting pin 4	default=1
8	DM3	I	Display mode setting pin 3	default=1
9	DM2	I	Display mode setting pin 2	default=1
10	DM1	I	Display mode setting pin 1	default=1
11	SDC	I	Color arrangement mode selection pin, Stripe=1, Delta=0	default=1
12	DLT	I	Delta mode selection pin	default=1

IC BLOCK DIAGRAM & DESCRIPTION

IC 8D02C

Pin	Name	I/O	Description	Remark
13	HPO	O	H-POS position adjustment output signal	
14	HPI	I	H-POS position adjustment input signal	
15	PDA	O	Phase detect A output pin	
16	CKC	I	Control HSY & VSY pin for select I/O direction	default=1
17	OSO	O	Oscillator output pin	
18	OSI	I	Oscillator input pin	
19	FD2	I	Master clock frequency divide by 2 function (FD2=0,/2)	default=1
20	NC1			
21	ZMI	I	Connect capacitor to ground	
22	ZMO	O	Connect Resistor to pin 21.	
23	CBG	I	Simultaneous CP2, CP3 sampling clock select pin	default=1
24	SAM	I	Simultaneous (1) or sequential (0) sampling select pin	default=0
25	RLC	I	Source driver shift right /left select pin	default=1
26	OEH	O	Source driver control signal	
27	SH2	O	Horizontal start pulse 2 for source driver (RLC=0,OUT)	
28	SH1	O	Horizontal start pulse 1 for source driver (RLC=0,OUT)	
29	CP3	O	Sampling clock 3 to source driver	
30	CP2	O	Sampling clock 2 to source driver	
31	CP1	O	Sampling clock 1 to source driver	
32	GND		Ground	
33.	VCC		Power supply	Note 1
34	Q1H	O	Source driver control signal	
35	RST	O	Vertical reset signal for source driver	
36	CPV	O	Scan clock to gate driver	
37	OE1	O	Gate driver Scan output enable control	
38	OE2	O	Gate driver scan output enable control	
39	OE3	O	Gate driver scan output enable control	
40	NC2			default=1
41	SV1	O	Vertical start pulse 1 for gate driver (UDC=1, OUT)	
42	SV2	O	Vertical start pulse 1 for gate driver (UDC=1, OUT)	
43	UDC	I	Up/down scan direction select pin	default=1
44	VP1	I	Vertical position adjustment for display area	default=0
45	VP2	I	Vertical position adjustment for display area	default=0
46	VP3	I	Vertical position adjustment for display area	default=0

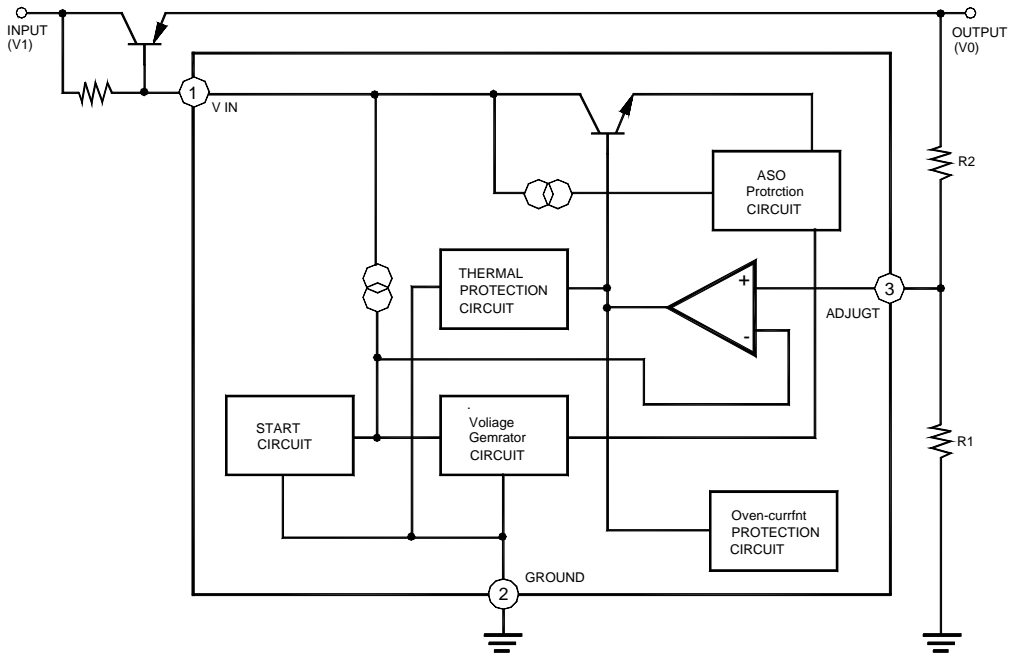
IC BLOCK DIAGRAM & DESCRIPTION

IC 8D02C

47	VP4	I	Vertical position adjustment for display area	default=1
48	POI	I	Power ON initialize; and UOB signal input	Note 3
49	POD	I	Power ON delay; VCO adjust can connect to GND.	Note 4
50	NC3			Note 5
51	NPC	O	NTSC/PAL detect output & Control pin, NTSC=1, PAL=0	Note 6
52	NC4			Note 5
53	G24	I	Gate 240=1 or 244=0 select pin	default=1
54	3OE	I	3 OEV=1 or 1 OEV=0 select pin	default=0
55	NC5			default=1
56	VSY	I/O	Vertical sync. input/Negative output pin	Pull high
57	HSY	I/O	Horizontal sync, input/Negative output pin	Pull high
58	BLK	O	Output for control RGB signal	
59	ESY	O	Output external sync. For control chroma decoder	
60	COM	O	Output VCOM polarity signal	
61	FRP	O	Video polarity alternating signal	
62	NC6			default=1
63	VIY	I	Vertical sync, input, if no use please connect to GND.	Note 2
64	GND		Ground	

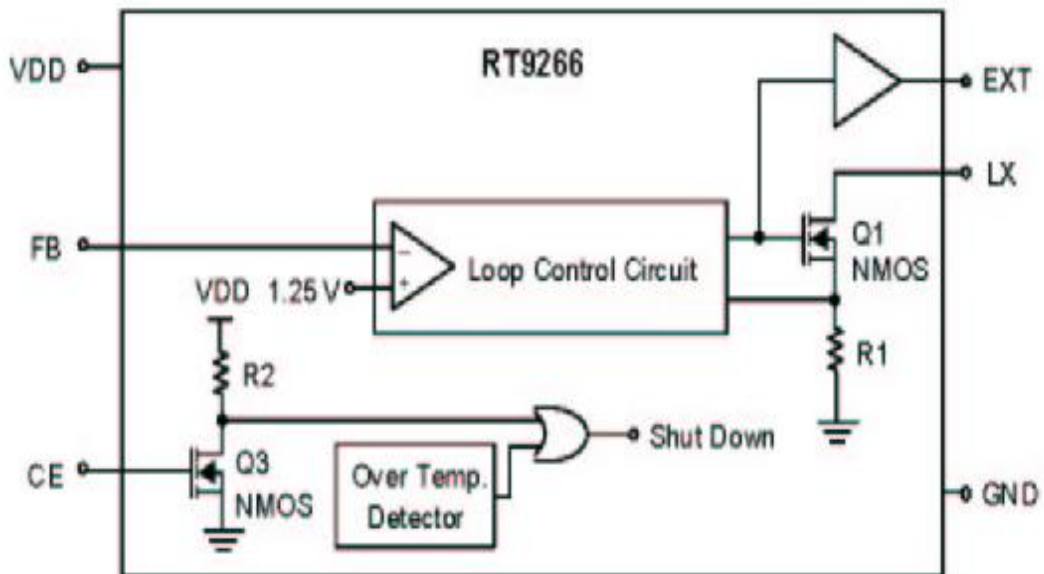
IC BLOCK DIAGRAM & DESCRIPTION

IC M5237



PIN	PIN NAME
1.	V IN
2.	GROUND
3.	ADJUST

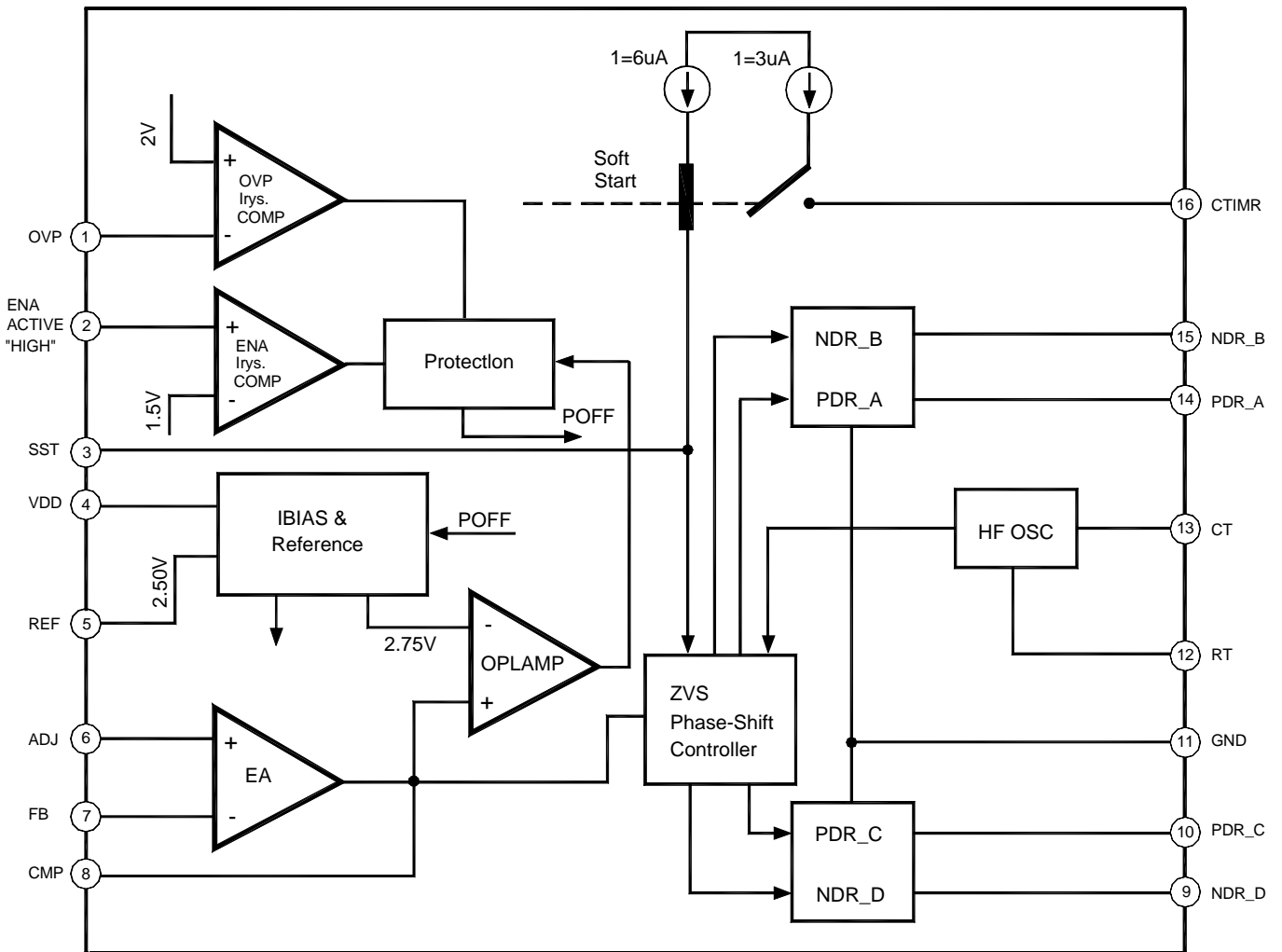
IC RT9266



PIN	PIN NAME	PIN	PIN NAME
1.	CE	4	LX
2.	EXT	5	VDD
3.	GND	6	FB

IC BLOCK DIAGRAM & DESCRIPTION

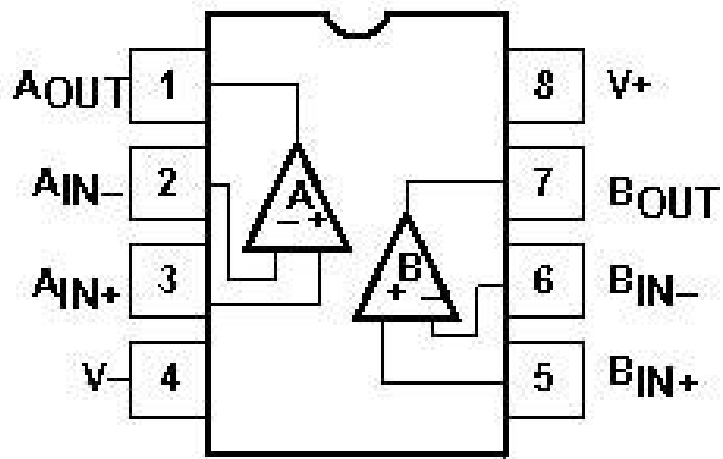
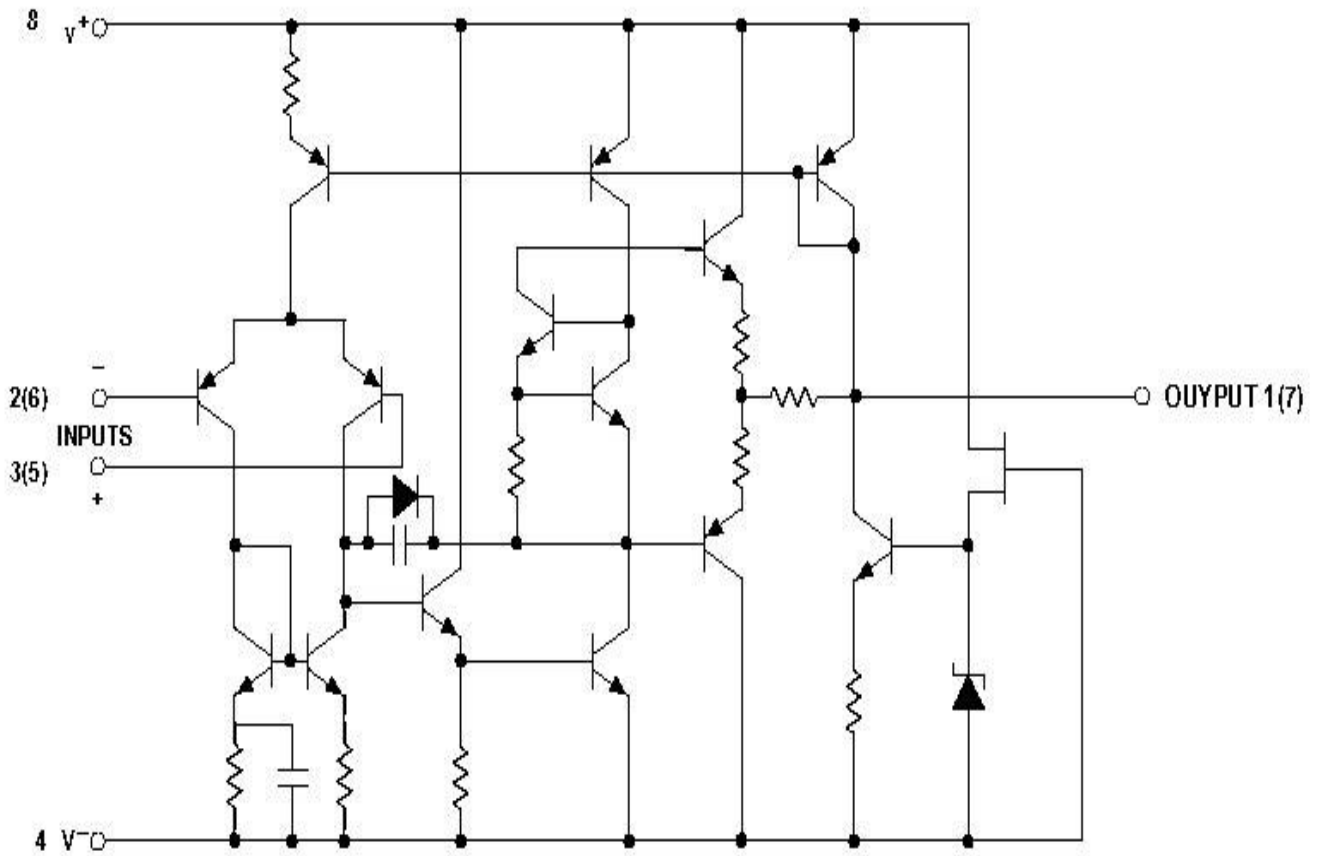
IC OZ970G



PIN	PIN NAME	PIN	PIN NAME
1.	OVP	9	NDR_D
2.	ENA ACTIVE "HIGH"	10.	PDR_C
3.	SST	11.	GND
4.	VDD	12.	RT
5.	REF	13.	CT
6.	ADJ	14.	PDR_A
7.	FB	15.	NDR_B
8.	CMP	16.	CTIMR

IC BLOCK DIAGRAM & DESCRIPTION

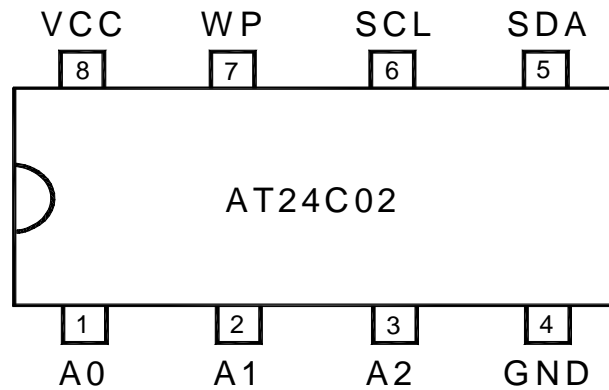
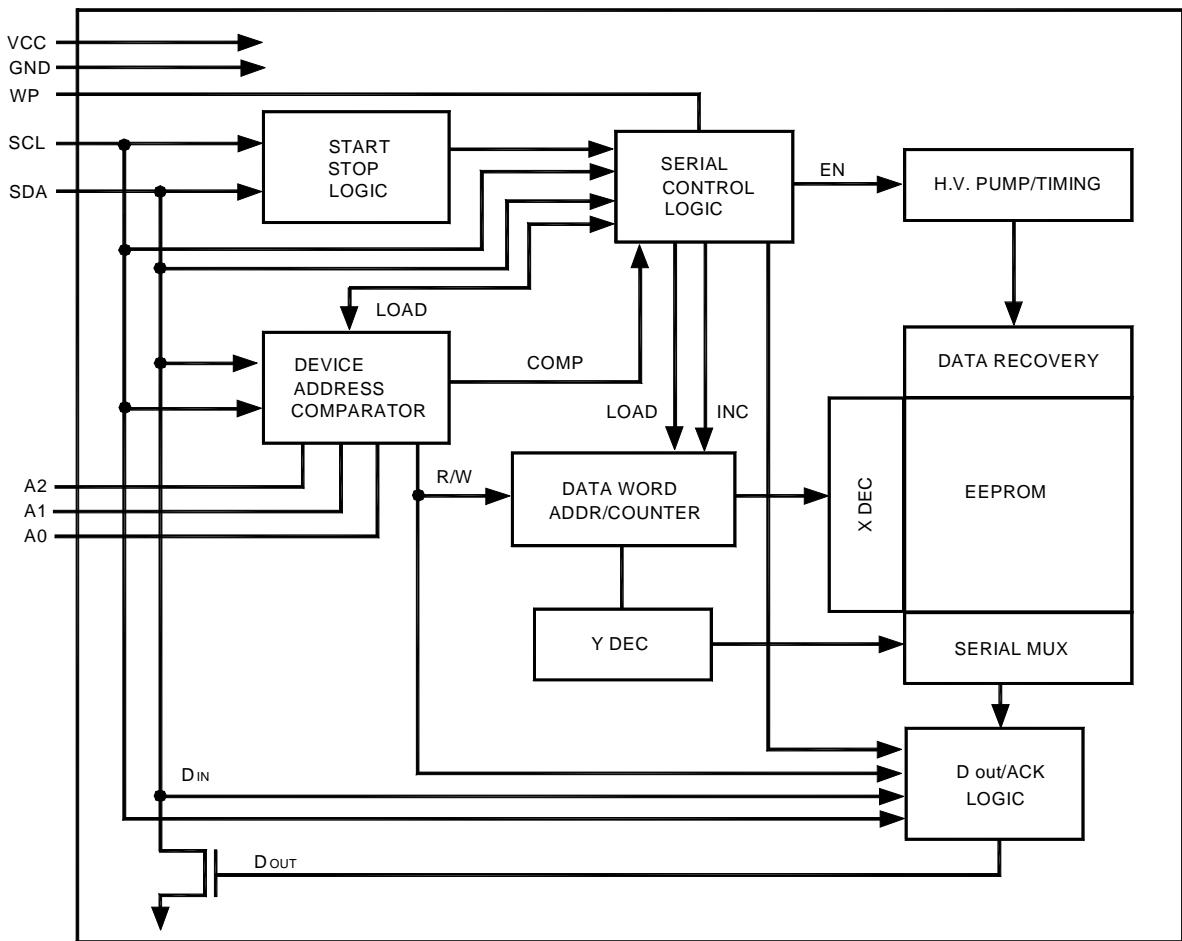
DVD IC 4558



PIN	NAME	PIN	NAME
1.	AOUT	5.	BIN+
2.	AIN-	6.	BIN-
3.	AIN+	7.	BOUT
4.	V-	8.	V+

IC BLOCK DIAGRAM & DESCRIPTION

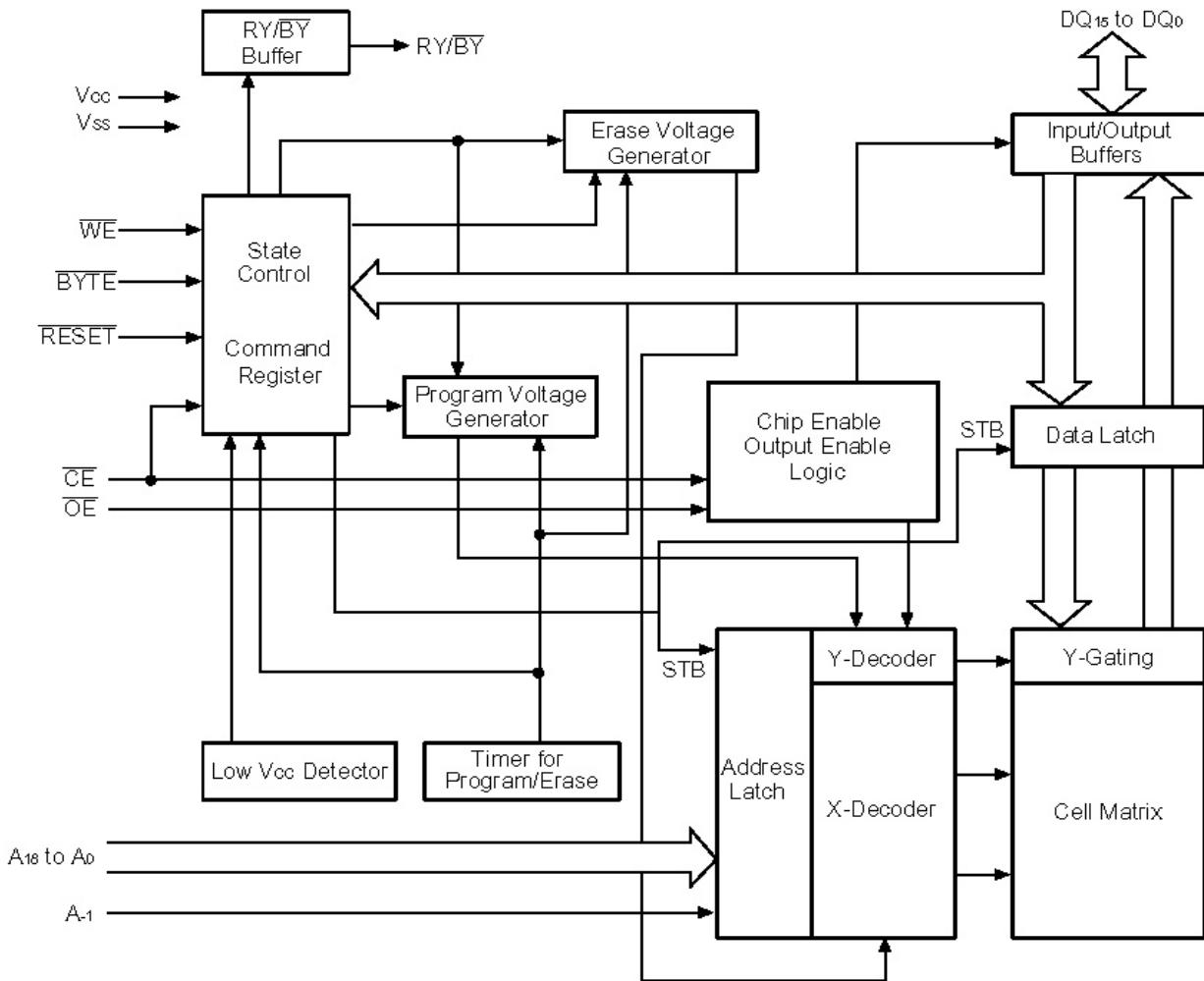
AT24C02



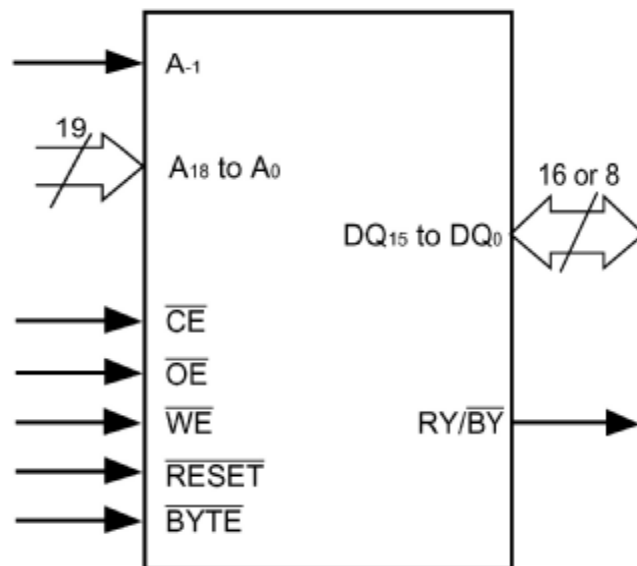
- | | | | |
|----|-----|----|-----|
| 1. | A0 | 5. | SDA |
| 2. | A1 | 6. | SCL |
| 3. | A2 | 7. | WP |
| 4. | GND | 8. | VCC |

IC BLOCK DIAGRAM & DESCRIPTION

U9 MBM29F800TA

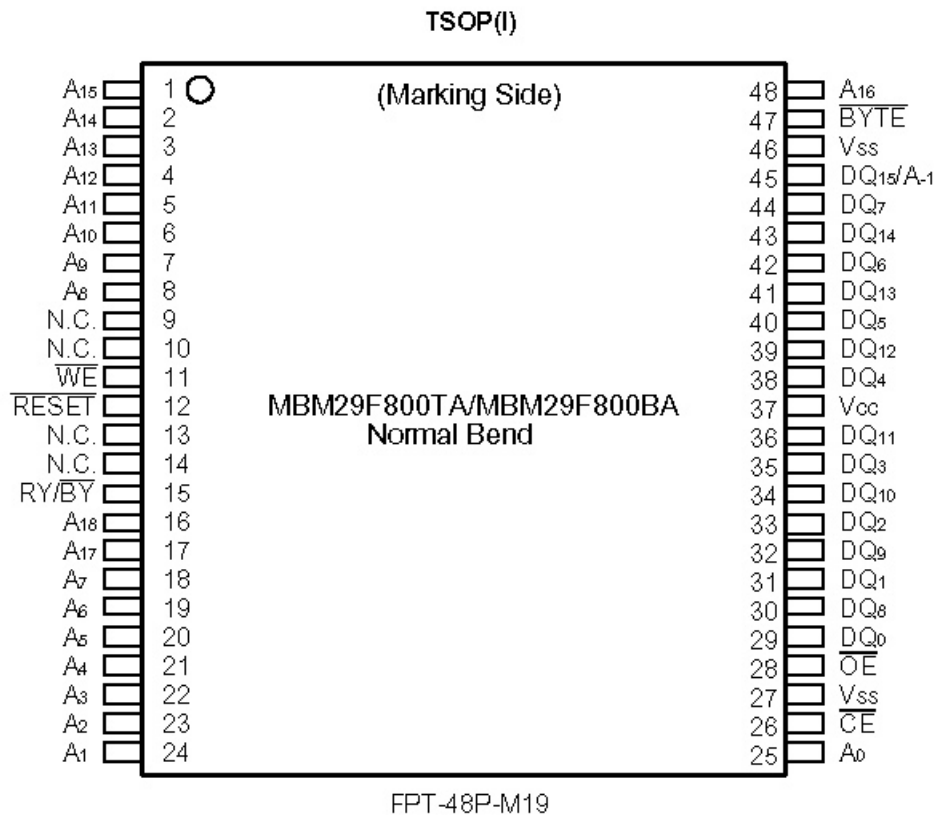


LOGIC SYMBOL



IC BLOCK DIAGRAM & DESCRIPTION

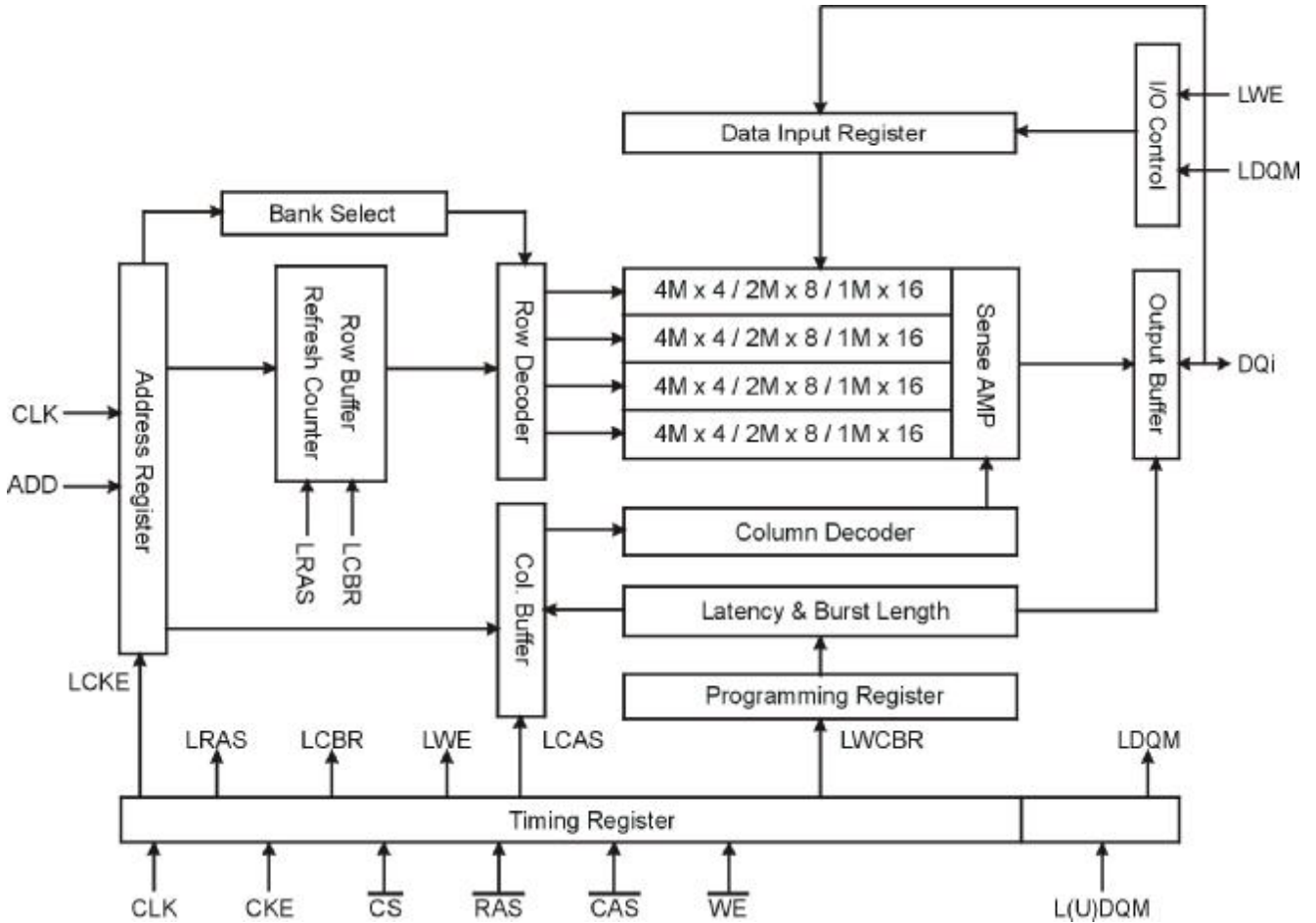
U9 MBM29F800TA



Pin Name	Function
A-1, A18 to A0	Address Inputs
DQ15 to DQ0	Data Inputs/Outputs
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{RY/BY}}$	Ready/Busy Output
$\overline{\text{RESET}}$	Hardware Reset Pin/Temporary Sector Unprotection
BYTE	Selects 8-bit or 16-bit mode
N.C.	No Internal Connection
Vss	Device Ground
Vcc	Device Power Supply

IC BLOCK DIAGRAM & DESCRIPTION

IC K4S641632



x16	x8	x4			x4	x8	x16
VDD	VDD	VDD	1	54	VSS	VSS	VSS
DQ0	DQ0	N.C	2	53	N.C	DQ7	DQ15
VDDQ	VDDQ	VDDQ	3	52	VSSQ	VSSQ	VSSQ
DQ1	N.C	N.C	4	51	N.C	N.C	DQ14
DQ2	DQ1	DQ0	5	50	DQ3	DQ6	DQ13
VSSQ	VSSQ	VSSQ	6	49	VDDQ	VDDQ	VDDQ
DQ3	N.C	N.C	7	48	N.C	N.C	DQ12
DQ4	DQ2	N.C	8	47	N.C	DQ5	DQ11
VDDQ	VDDQ	VDDQ	9	46	VSSQ	VSSQ	VSSQ
DQ5	N.C	N.C	10	45	N.C	N.C	DQ10
DQ6	DQ3	DQ1	11	44	DQ2	DQ4	DQ9
VSSQ	VSSQ	VSSQ	12	43	VDDQ	VDDQ	VDDQ
DQ7	N.C	N.C	13	42	N.C	N.C	DQ8
VDD	VDD	VDD	14	41	VSS	VSS	VSS
<u>LDQM</u>	<u>N.C</u>	<u>N.C</u>	15	40	N.C/RFU	N.C/RFU	N.C/RFU
<u>WE</u>	<u>WE</u>	<u>WE</u>	16	39	DQM	DQM	UDQM
<u>CAS</u>	<u>CAS</u>	<u>CAS</u>	17	38	CLK	CLK	CLK
<u>RAS</u>	<u>RAS</u>	<u>RAS</u>	18	37	CKE	CKE	CKE
CS	CS	CS	19	36	N.C	N.C	N.C
BA0	BA0	BA0	20	35	A11	A11	A11
BA1	BA1	BA1	21	34	A9	A9	A9
A10/AP	A10/AP	A10/AP	22	33	A8	A8	A8
A0	A0	A0	23	32	A7	A7	A7
A1	A1	A1	24	31	A6	A6	A6
A2	A2	A2	25	30	A5	A5	A5
A3	A3	A3	26	29	A4	A4	A4
VDD	VDD	VDD	27	28	VSS	VSS	VSS

54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

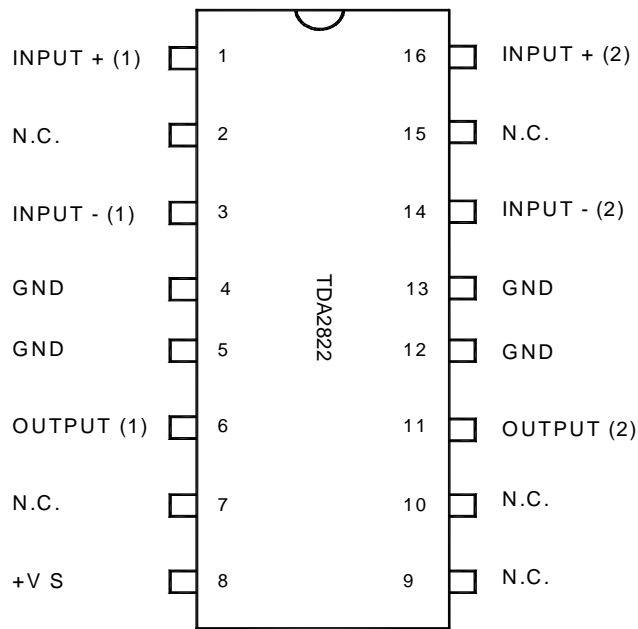
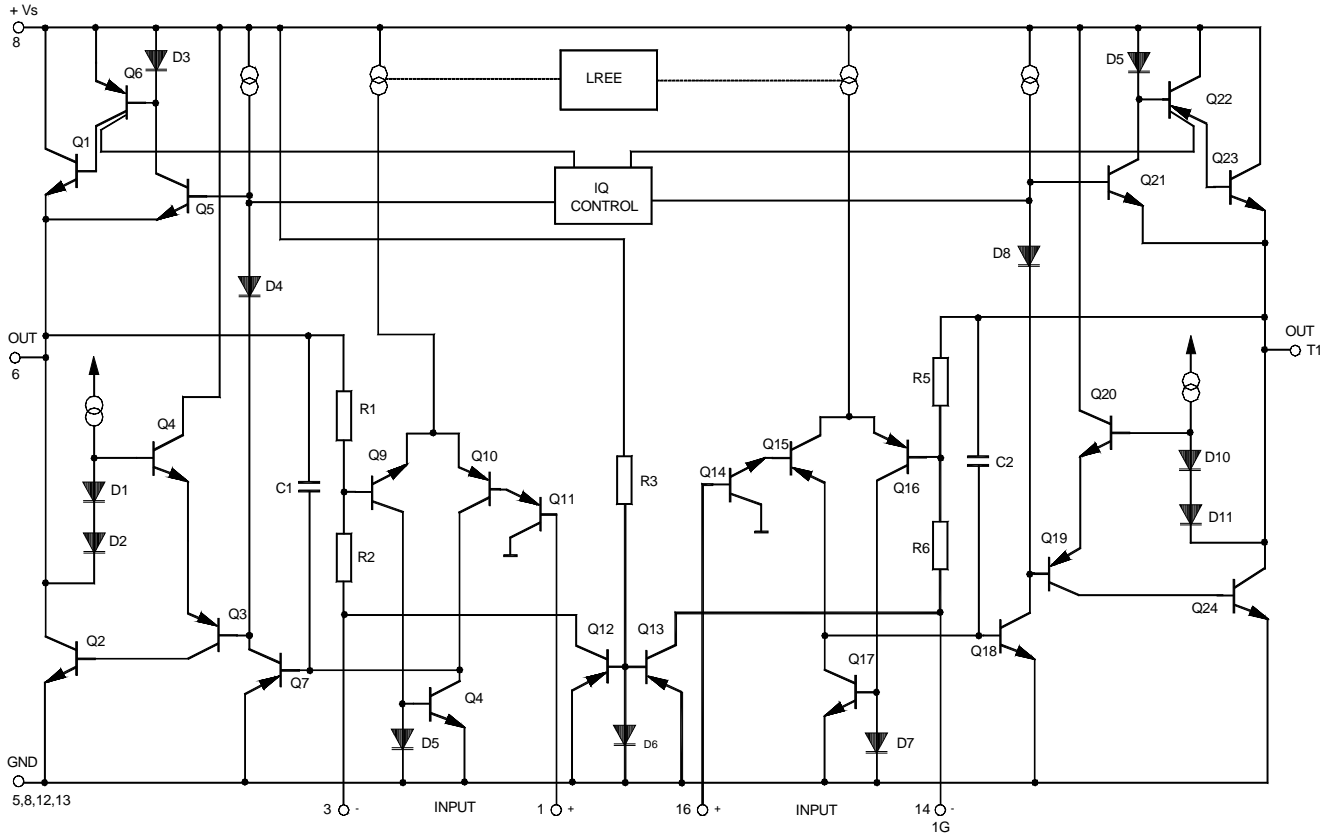
IC BLOCK DIAGRAM & DESCRIPTION

IC K4S641632

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A ₀ ~ A ₁₁	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA ₀ ~ RA ₁₁ , Column address : (x4 : CA ₀ ~ CA ₃ , x8 : CA ₀ ~ CA ₇ , x16 : CA ₀ ~ CA ₇)
BA ₀ ~ BA ₁	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active.
DQM	<i>Data input/output mask</i>	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active.
DQ ₀ ~ x ₁₅	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
V _{DD} /V _{SS}	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.
V _{DDQ} /V _{SSQ}	<i>Data output power/ground</i>	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C./RFU	<i>No connection /reserved for future use</i>	This pin is recommended to be left No Connection on the device.

IC BLOCK DIAGRAM & DESCRIPTION

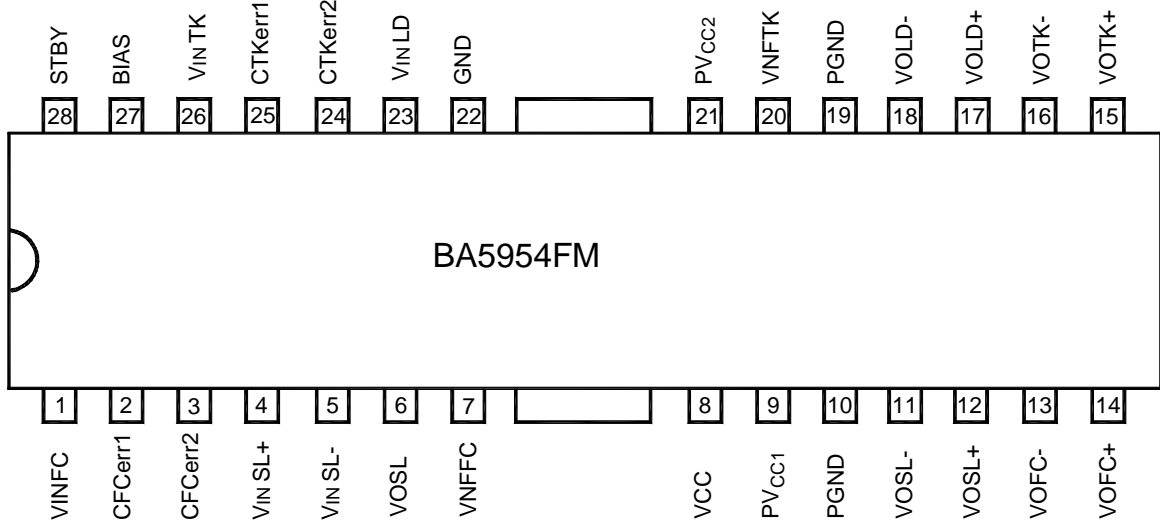
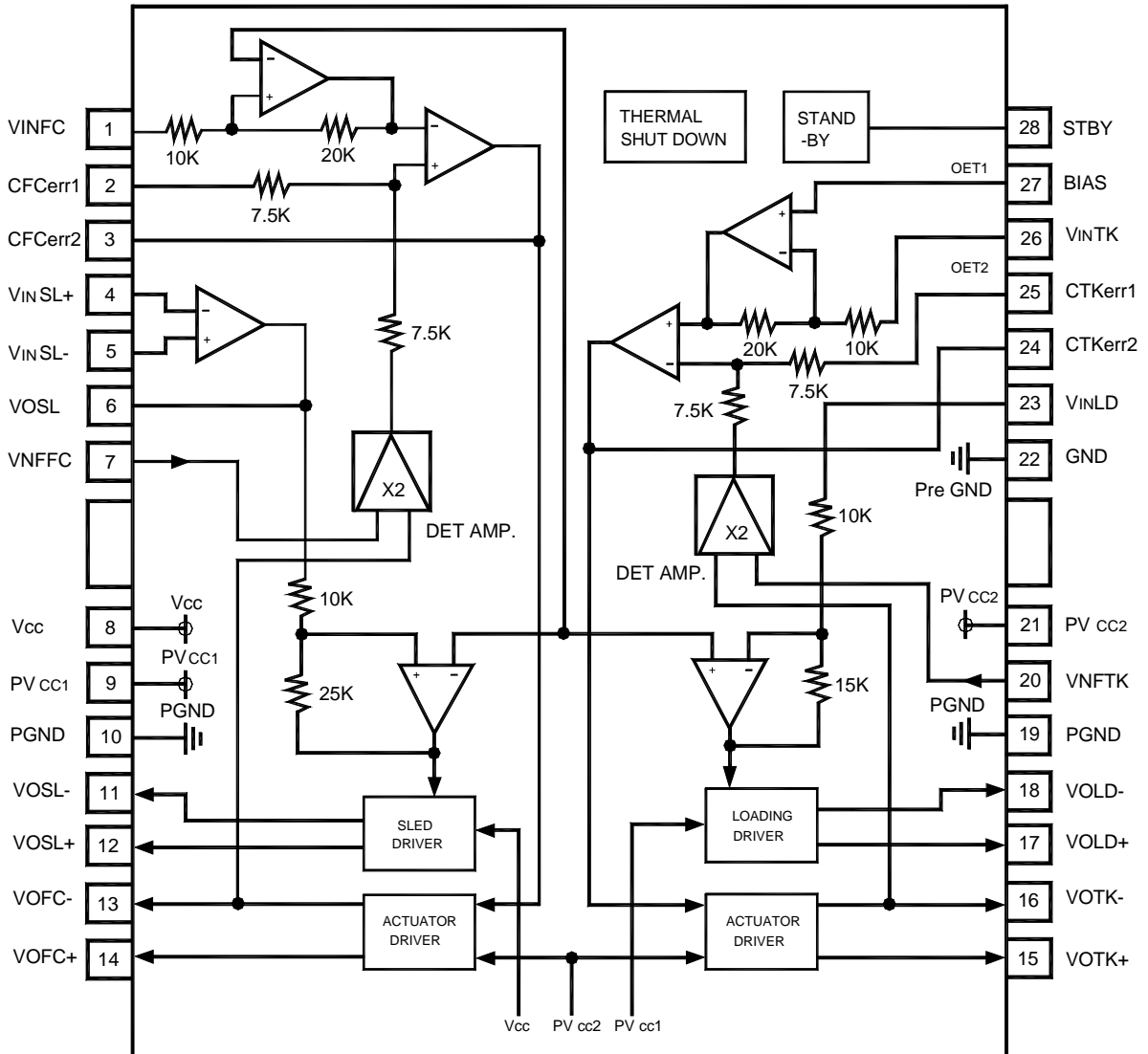
U2 TDA2822



- | | | | |
|----|------------|-----|-------------|
| 1. | INPUT +(1) | 9. | N.C. |
| 2. | N.C. | 10. | N.C. |
| 3. | INPUT -(1) | 11. | OUTPUT (2) |
| 4. | GND | 12. | GND |
| 5. | GND | 13. | GND |
| 6. | OUTPUT (1) | 14. | INPUT - (2) |
| 7. | N.C. | 15. | N.C. |
| 8. | +V5 | 16. | INPUT + (2) |

IC BLOCK DIAGRAM & DESCRIPTION

U18 BA5954

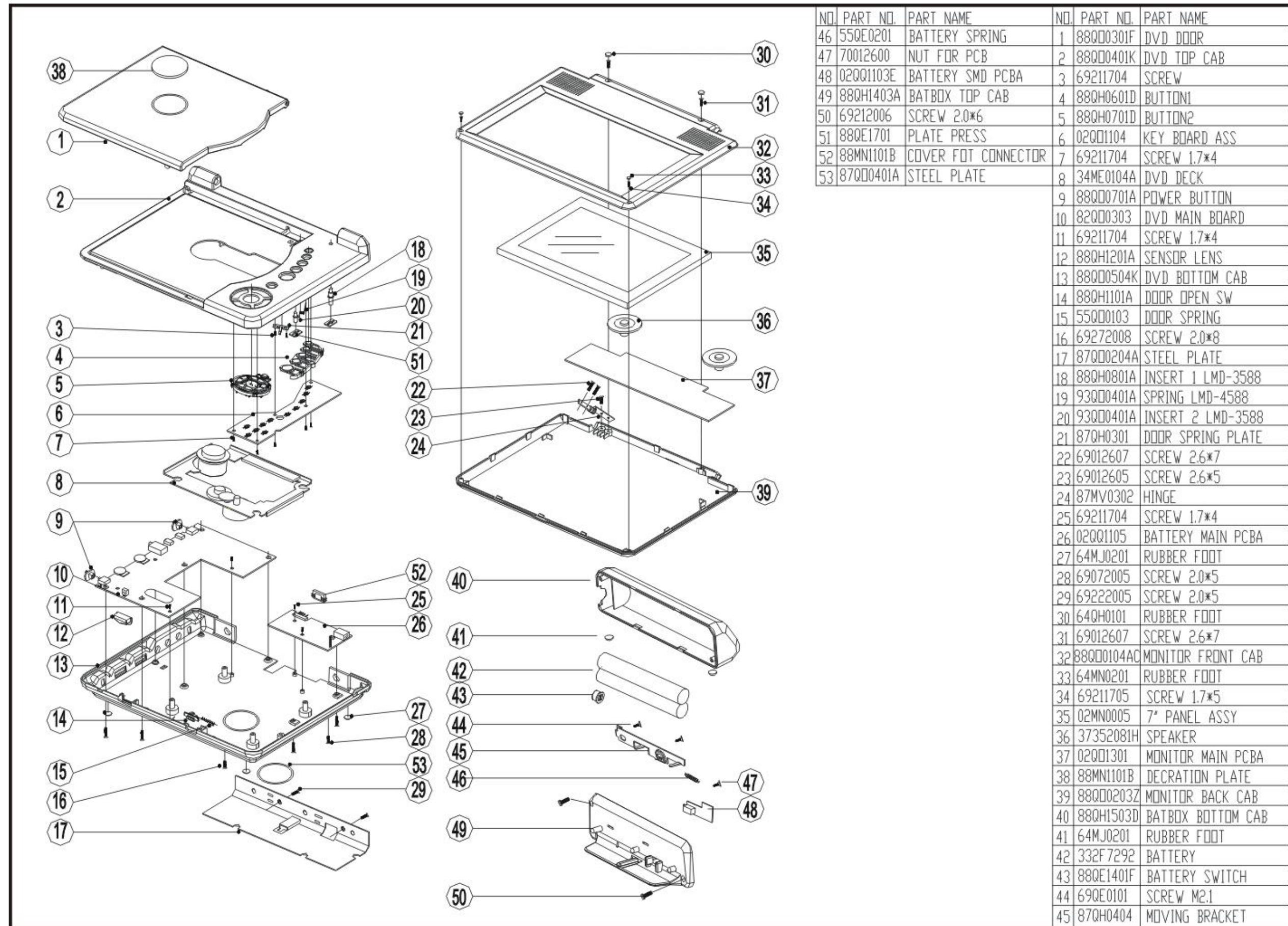


IC BLOCK DIAGRAM & DESCRIPTION

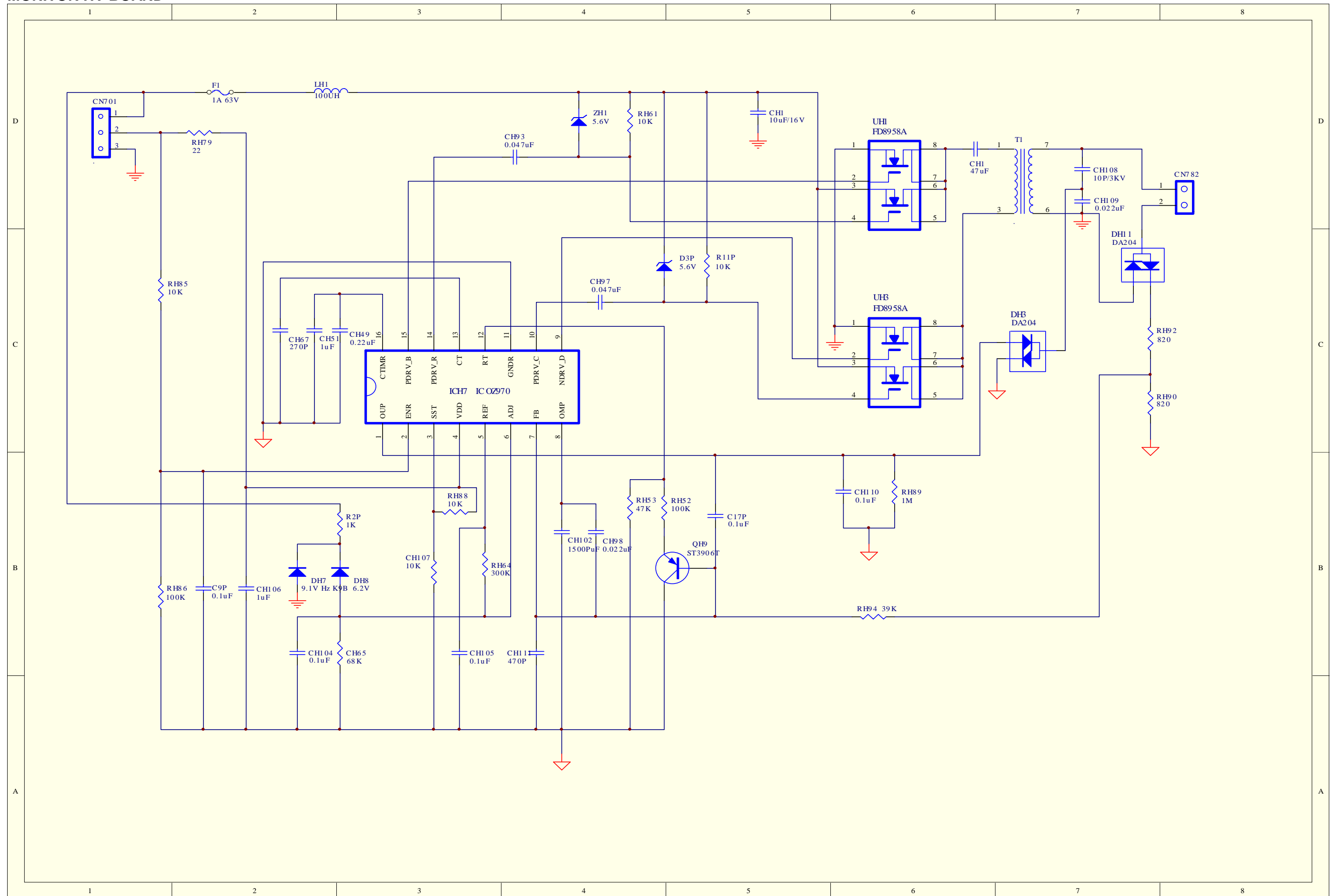
U18 BA5954FM

Pin No.	Pin name	Function
1.	VINFC	Focus drive input
2.	CFC err1	For connection of capacitor for the error amp filter
3.	CFC err2	For connection of capacitor for the error amp filter
4.	VINSL +	Op-amp input (+) for the sled driver
5.	VINSL -	Op-amp input (-) for the sled driver
6.	VOSL	Op-amp output for the sled driver
7.	VNFFC	Focus driver feedback pin
8.	Vcc	VCC
9.	PV cc1	Power Vcc for sled driver block
10.	PGND	Ground for Sled Driver block
11.	VOSL -	Sled driver output (-)
12.	VOSL +	Sled driver output (+)
13.	VOFC -	Focus driver output (-)
14.	VOFC +	Focus driver output (+)
15.	VOTK +	Tracking driver output (+)
16.	VOTK -	Tracking driver output (-)
17.	VOLD +	Loading driver output (+)
18.	VOLD -	Loading driver output (-)
19.	PGND	Ground for Actuator driver block
20.	VNFTK	Tracking driver feedback pin
21.	PV cc2	Power Vcc for Actuator driver block
22.	GND	Ground
23.	VINTK	Loading driver input
24.	CTKerr2	For connection of capacitor for the error amp filter
25.	CTKerr1	For connection of capacitor for the error amp filter
26.	VINTK	Tracking driver input
27.	BLAS	Bias input
28.	STBY	Stand – By control

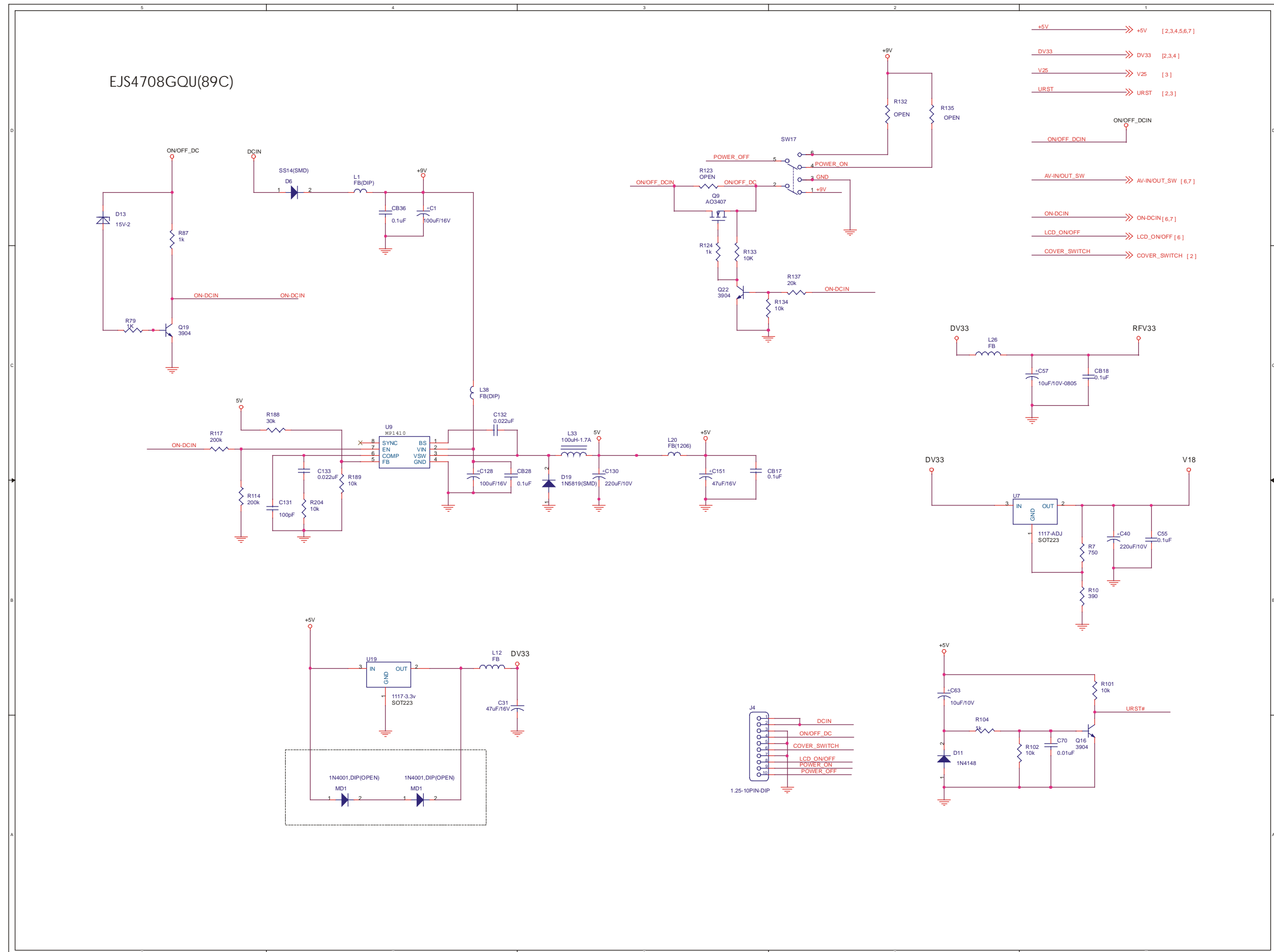
EXPLODED VIEW

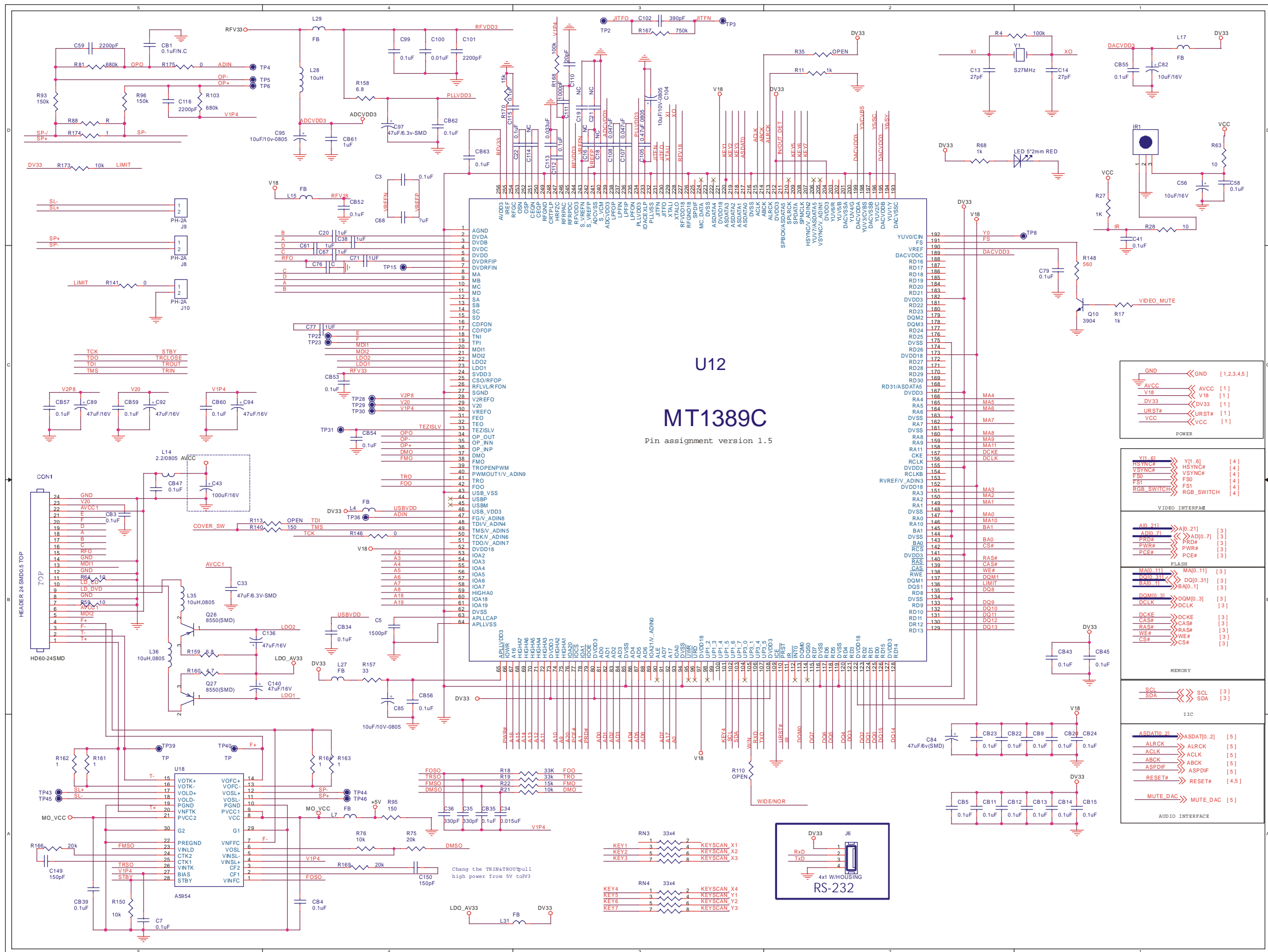


**MONITOR PART
MONITOR HV BOARD**

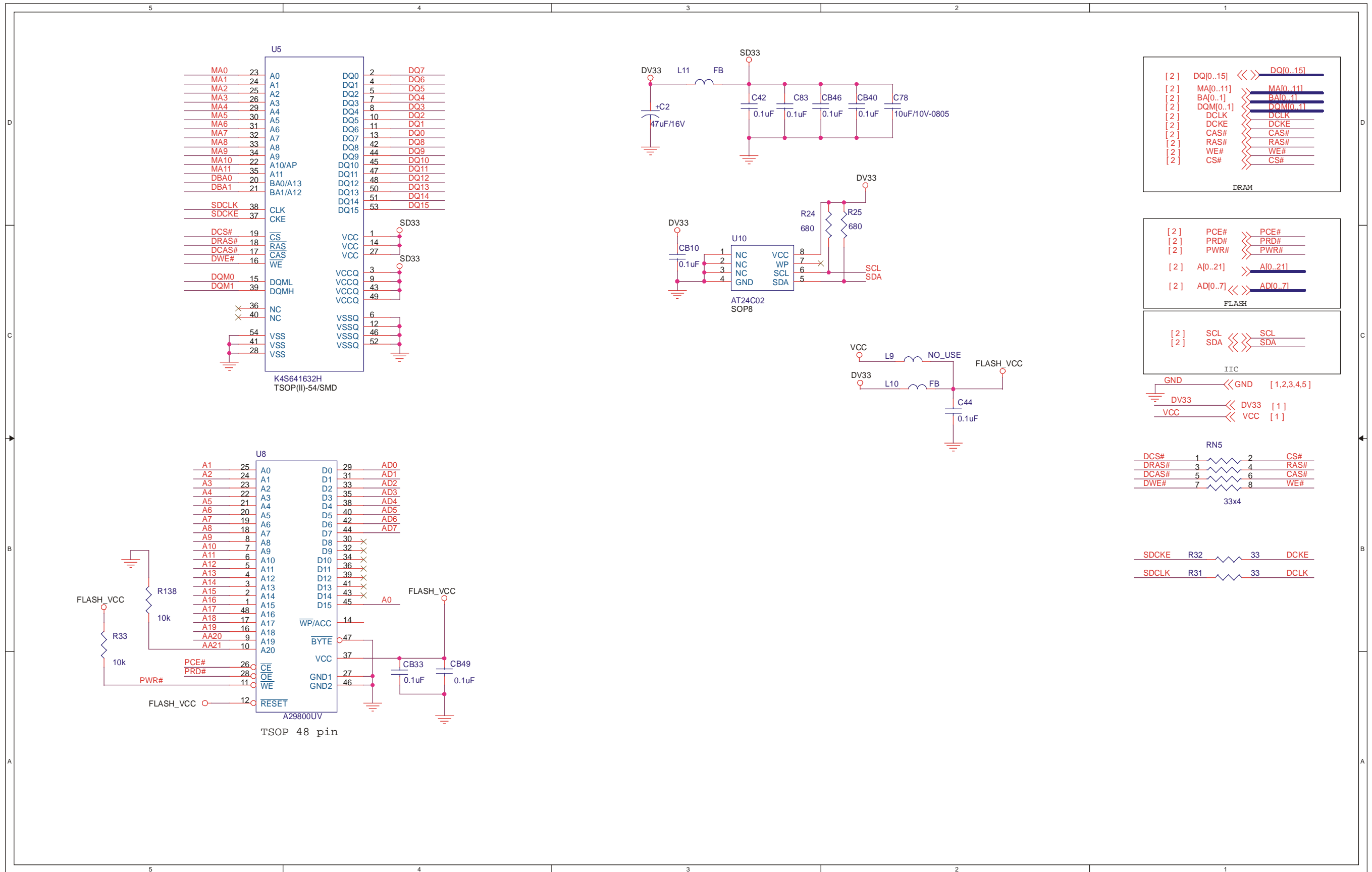


DVD Part
DVD POWER

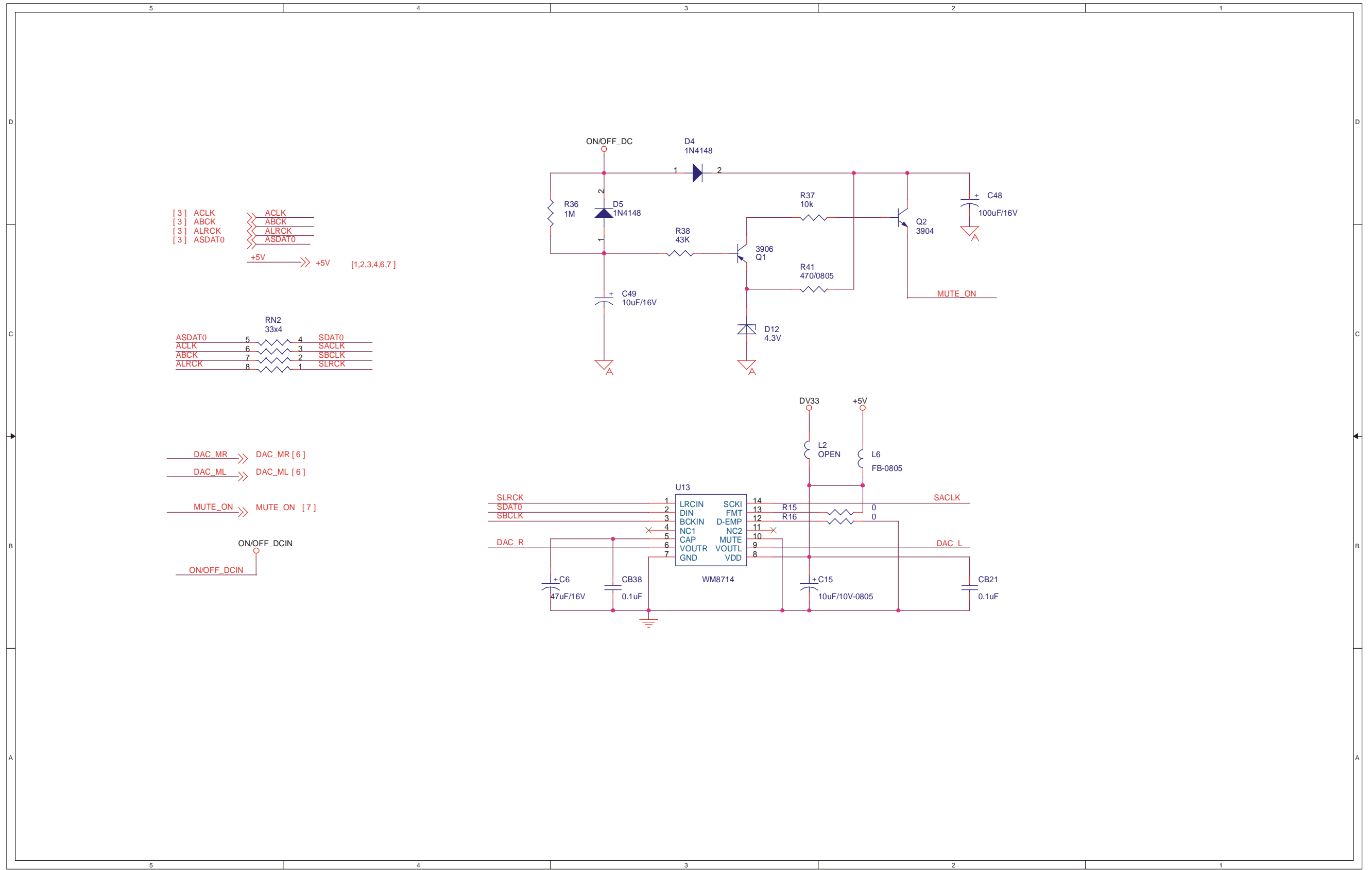




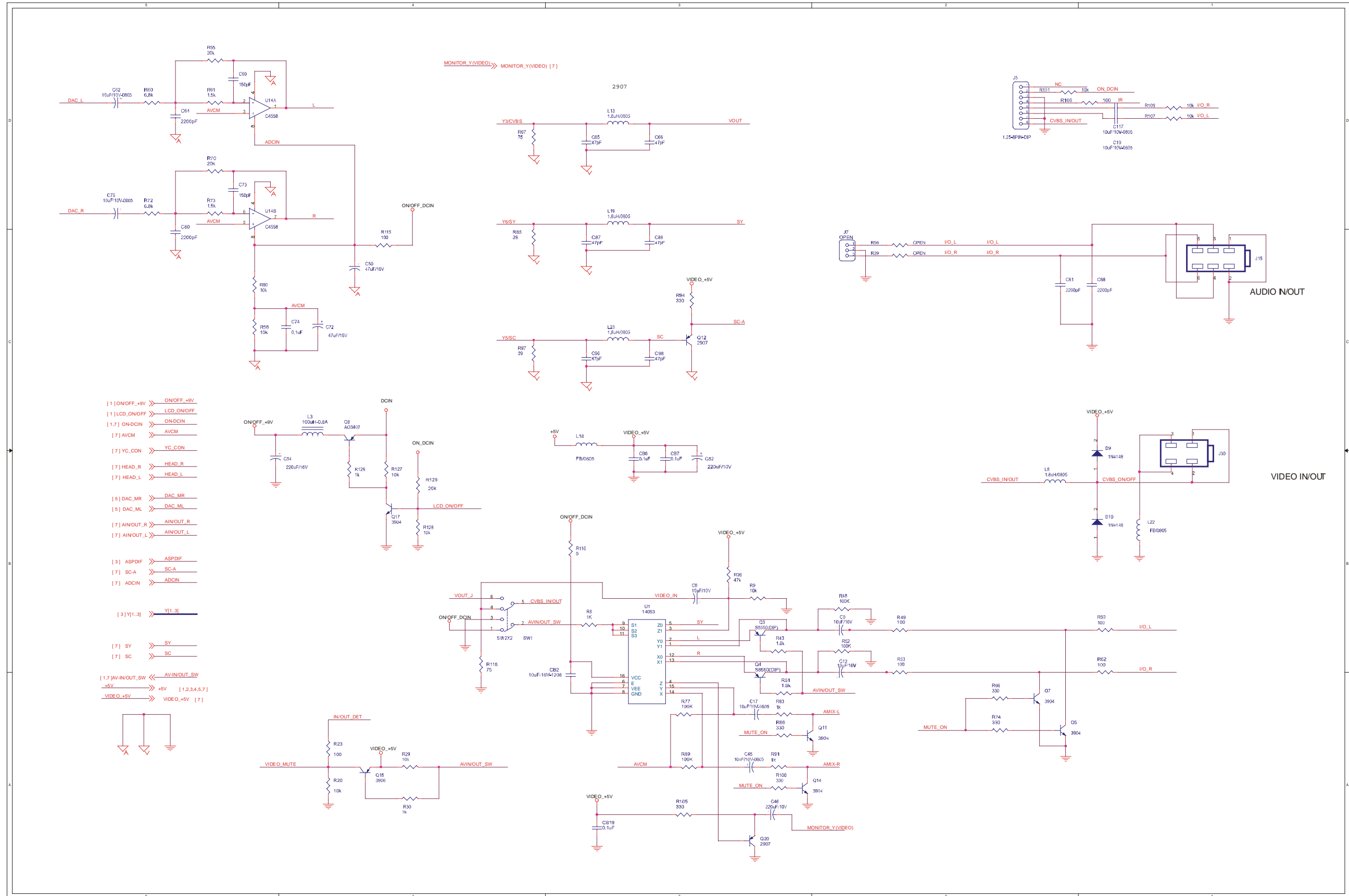
DVD ROM & RAM



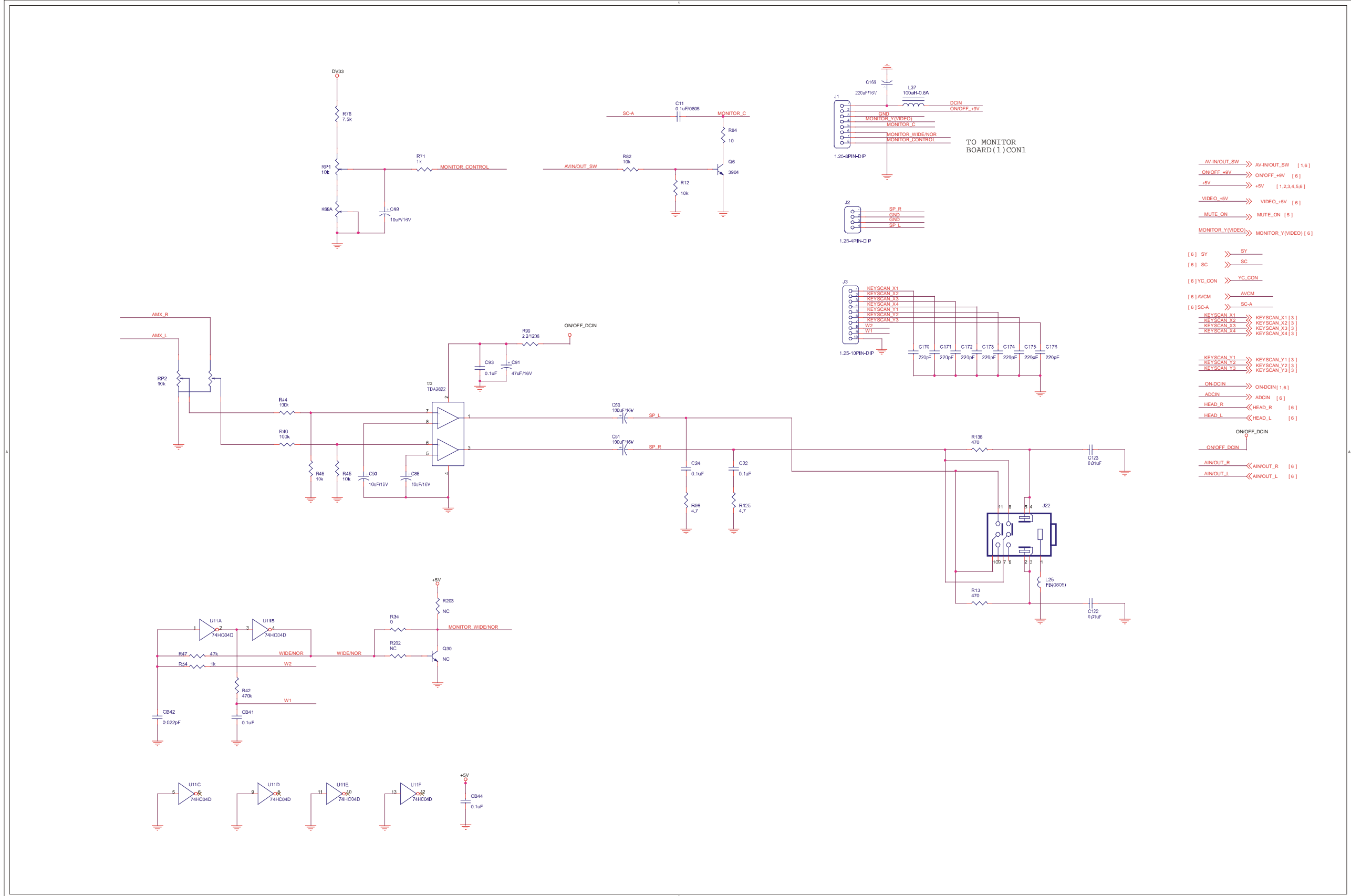
DVD MUTE



DVD AV



DVD AUDIO JACK



- AV-IN/OUT_SW >> AV-IN/OUT_SW [1,6]
- ON/OFF_+9V >> ON/OFF_+9V [6]
- +5V >> +5V [1,2,3,4,5,6]
- VIDEO_+5V >> VIDEO_+5V [6]
- MUTE_ON >> MUTE_ON [5]
- MONITOR_Y(VIDEO) >> MONITOR_Y(VIDEO) [6]
- [6] SY >> SY
- [6] SC >> SC
- [6] YC_CON >> YC_CON
- [6] AVCM >> AVCM
- [6] SC-A >> SC-A
- KEYSCAN_X1 >> KEYSCAN_X1 [3]
- KEYSCAN_X2 >> KEYSCAN_X2 [3]
- KEYSCAN_X3 >> KEYSCAN_X3 [3]
- KEYSCAN_X4 >> KEYSCAN_X4 [3]
- KEYSCAN_Y1 >> KEYSCAN_Y1 [3]
- KEYSCAN_Y2 >> KEYSCAN_Y2 [3]
- KEYSCAN_Y3 >> KEYSCAN_Y3 [3]
- ON/DCIN >> ON/DCIN [1,6]
- ADCIN >> ADCIN [6]
- HEAD_R >> HEAD_R [6]
- HEAD_L >> HEAD_L [6]
- ON/OFF_DCIN
- AINOUT_R >> AINOUT_R [6]
- AINOUT_L >> AINOUT_L [6]

MEMO

A large empty rectangular box with a black border, intended for writing the memo content.